HOLT INTEGRATED CIRCUITS

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HI-6120 Parallel Bus Interface and HI-6121 Serial Peripheral Interface (SPI) MIL-STD-1553 Remote Terminal ICs

GENERAL DESCRIPTION

The HI-6120 and HI-6121 provide a complete, integrated, 3.3V MIL-STD-1553 Remote Terminal in a monolithic silicon gate CMOS device. Two host interface options are offered: The HI-6120 uses a 16-bit parallel host bus interface for access to registers and RAM and is offered in a 100-pin plastic quad flat pack (PQFP). The HI-6121 has a 4-wire SPI (Serial Peripheral Interface) host connection and comes in a reduced pin count 52-pin PQFP or 9mm x 9mm 64-pin QFN. Both devices handle all aspects of the MIL-STD-1553 protocol, including message encoding, decoding, error detection, illegal command detection and data buffering. Host data management is simplified by storing message information and data within the on-chip 32K x 16 static RAM.

A descriptor table in shared RAM provides fully programmable memory management. Multiple descriptor tables can be implemented for fast context switching. Transmit and receive commands can use any of four different data buffer modes: indexed (single) buffering, ping-pong (double) buffering or two circular buffer schemes. Transmit and receive commands for each subaddress may use different buffer modes. Mode code commands employ a simple scheme for storing mode data and message information with programmable interrupts.

The device provides internal illegalization capability, allowing any subset of subaddress, command T/$\overline{R}$ bit, broadcast vs non-broadcast and word count (or mode code) to be illegalized, resulting in a total of 4,096 possible combinations. The illegalization table resides in internal RAM. The RT can also operate without illegal command detection, providing “in form” responses to all valid commands. Broadcast command recognition is optional.

The HI-6120 and HI-6121 provide programmable interrupts for automatic message handling, message status and general status. A host interrupt history log maintains information about the last 16 interrupts.

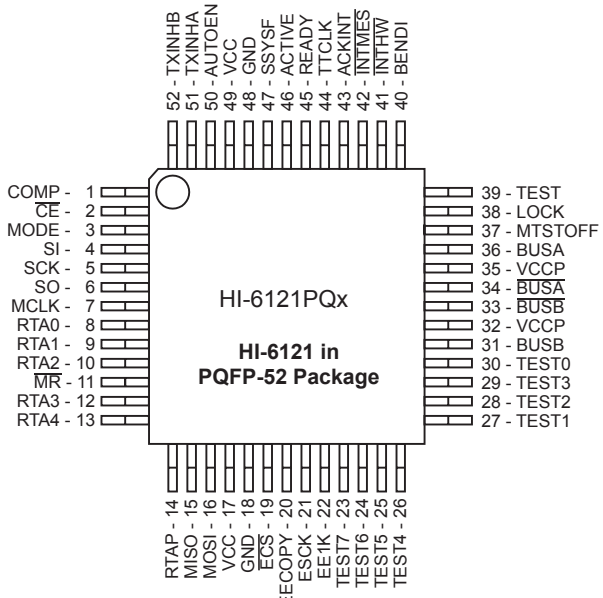
The HI-6120 and HI-6121 can be configured for automatic self-initialization. A dedicated SPI port reads data from external serial EEPROM memory to fully configure the descriptor table, illegalization table and host interrupts.

Internal dual-redundant transceivers provide direct connection to bus isolation transformers. The device is offered with industrial temperature range as well as extended temperature range with optional burn-in. A “RoHS compliant” lead-free option is also offered.

FEATURES

- Fully integrated 3.3V Remote Terminal meets all requirements for MIL-STD-1553B Notice 2
- Four data buffer modes for subaddress transmit and receive commands. Data buffer modes are independently selectable for transmit and receive commands on each subaddress
- Simplified mode code command handling
- Integral 16-bit Time-Tag counter has programmable options for clock, interrupts and auto-synchronization
- Message information and time-tag words are stored with message data words for all transacted messages
- In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data
- Optional interrupt log buffer stores the most recent 16 interrupts to minimize host service duties
- Optional illegal command detection uses internal table
- Optional automatic self-initialization at reset
- ±8kV ESD Protection (HBM, all pins)
- MIL-STD-1760 compliant

PIN CONFIGURATION (TOP)



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1. BLOCK DIAGRAM

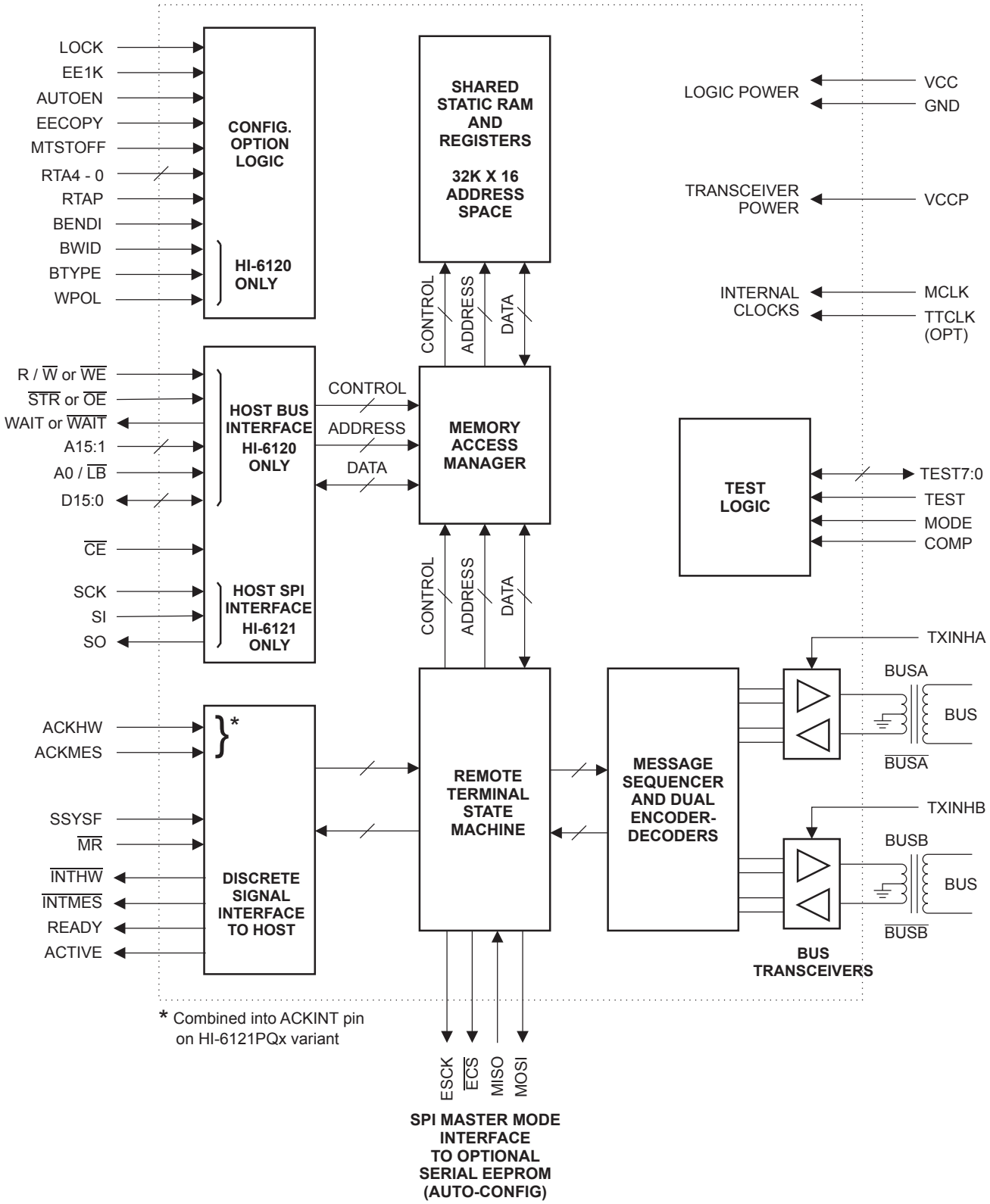


Figure 1. HI-6120 / HI-6121 Block Diagram

2. PIN DESCRIPTIONS

Table 1. Pin Descriptions (Both HI-6120 and HI-6121)

Pin	Function	Description
$\overline{\text{INTHW}}$	OUTPUT	Hardware Interrupt output, active low.This signal is programmed as a brief low-going pulse output, or as a level output by the INTSEL bit in Configuration Register 1.
$\overline{\text{INTMES}}$	OUTPUT	Message Interrupt output, active low. This signal is programmed as a brief low-going pulse output, or as a level output by the INTSEL bit in Configuration Register 1.
$\overline{\text{MR}}$	INPUT	Master Reset, active low. Internal 50kΩ pull-up resistor. The host can also assert software reset by setting the SRST bit in Configuration Register 1.
MTSTOFF	INPUT	Memory test disable, active high. Internal 50kΩ pull-down resistor. When this pin is low, the device performs a memory test on the entire RAM after rising edge on the $\overline{\text{MR}}$ reset pin. When this pin is high, the RAM test is skipped, resulting in a faster reset process. For further information, refer to Section 14 on page 103.
EECOPY	INPUT	EEPROM Copy, active high. Internal 50kΩ pull-down resistor. This input is used to start the process that copies registers and configuration tables to serial EEPROM. Refer to Section 14 on page 103.
AUTOEN	INPUT	Auto-Initialize Enable, active high. Internal 50kΩ pull-down resistor. If this pin is high at rising edge on $\overline{\text{MR}}$ reset input, automatic initialization proceeds, copying configuration data to registers and RAM from an external serial EEPROM via the dedicated auto-initialization SPI port. Refer to Section 14 on page 103**.**
EE1K	INPUT	When the AUTOEN pin is high, the EE1K input sets the range of the auto-initialization process. When EE1K is low, registers and RAM occupying the 32K address range from 0x0 to 0x7FFF are initialized. For applications needing faster initialization, when EE1K is high, only registers and RAM occupying the 1K address range from 0x0 to 0x03FF are initialized. This pin has an internal 50kΩ pull-down resistor. If the AUTOEN pin is low, this pin is not used. Refer to Section 14 on page 103**.**
RTA4:0 RTAP	INPUTS	Remote terminal address bits 4 - 0, and parity bit. Internal 50kΩ pull-up resistors. The RTAP pin should provide odd parity for the address present on pins RTA4:0. Terminal address and parity pin levels are latched into the Operational Status register when rising edge occurs on the $\overline{\text{MR}}$ pin. The Operational Status Register value (not these pins) reflects the active terminal address. The register value can be overwritten by the host under some circumstances. See section 5.3 on page 28.
LOCK	INPUT	Internal 50kΩ pull-down resistor. Pin state is latched into the Operational Status register LOCK bit when rising edge occurs on the $\overline{\text{MR}}$ pin. If Operational Status register LOCK bit is high, terminal address in the register cannot be overwritten by a host register write. If Operational Status register LOCK bit is low, the host can overwrite the five terminal address bits and address parity bit in the Operational Status register.
TXINHA TXINHB	INPUTS	Transmit Inhibits for Bus A and Bus B, active high. Internal 50kΩ pull-down resistors. These inputs are logically ORed with the corresponding TXINHA and TXINHB bits in Configuration Register 1. If the input pin or register bit is high, bus transmit is disabled.

Pin	Function	Description
READY	OUTPUT	Pin is low when auto-initialization or built-in test is in-process. **The host must not access shared RAM or device registers when pin state is low.** When output is high, the shared RAM and registers may be configured, and device will begin terminal execution when the STEX (start execution) bit in Configuration Register 1 is set.
ACTIVE	OUTPUT	Pin is high when the HI-6120 / HI-6121 is actively processing a valid MIL-STD-1553 command, otherwise low. The falling edge signifies message completion.
MCLK	INPUT	Master clock input, 50.0 MHz ±0.01% (100ppm). Internal 50kΩ pull-down resistor.
TTCLK	INPUT	Time-Tag Clock input. Internal 50kΩ pull-down resistor. When Configuration Register 1 bits TTCK2:0 = 001, this pin is the clock input for the Time Tag counter. For other values of TTCK2:0, the Time-Tag counter is internally clocked so the TTCLK pin is not used.
SSYSF	INPUT	Subsystem fail input, active high. Internal 50kΩ pull-down resistor. When this input is high, the HI-6120 / HI-6121 terminal sets the SUBSYS flag in its status word.
$\overline{\text{ECS}}$	OUTPUT	Chip select output for the dedicated Serial Peripheral Interface (SPI) that connects to the optional external serial EEPROM used for automatic self-initialization. For this auto-initialization SPI, the device operates in SPI master mode while the external memory operates in slave mode. This SPI is separate from the host SPI found in the HI-6121.
ESCK	OUTPUT	Serial Clock output signal for the dedicated auto-initialization SPI connected to external auto-initialization EEPROM.
MISO	INPUT	Serial Input signal (Master-In Slave-Out) for the dedicated auto-initialization SPI connected to external auto-initialization EEPROM. Internal 50kΩ pull-down resistor.
MOSI	OUTPUT	Serial Output signal (Master-Out Slave-In) for the dedicated auto-initialization SPI connected to external auto-initialization EEPROM.
BUSA, $\overline{\text{BUSA}}$	ANALOG	Bi-directional analog interface to MIL-STD-1553 bus A isolation transformer, positive and negative signals respectively.
BUSB, $\overline{\text{BUSB}}$	ANALOG	Bi-directional analog interface to MIL-STD-1553 bus B isolation transformer, positive and negative signals respectively.
VCC, VCCP	POWER	3.3V supply voltage inputs for logic and transceiver circuits.
GND	POWER	Ground pin for logic and transceiver circuits.
TEST	INPUT	Test enable. Internal 50kΩ pull-down resistor. The host asserts this pin to perform RAM self-test or loopback tests.
TEST7:0	BI-DIR	Test pins used for factory testing. Internal 50kΩ pull-down resistor. Do not connect these pins.
MODE	INPUT	Test pin used for factory testing. Internal 50kΩ pull-up resistor. Do not connect this pin.
COMP	INPUT	Test pin used for factory testing. Internal 50kΩ pull-down resistor. Do not connect this pin.

Pin	Function	Description
$\overline{CE}$	INPUT	Chip Enable, active low. Internal 50kΩ pull-up resistor. When asserted, this pin enables host read or write accesses to device RAM or registers. On HI-6121, it is normally connected to a host SPI slave select output signal.
BENDI	INPUT	Big Endian Configuration Pin Internal 50kΩ pull-up resistor. The BENDI pin works in conjunction with the A0 and BWID pins to determine the "endianness" or byte order of 16-bit word transfers to the HI-6120. Table 4 below summarizes the interoperability of the three pins. When using the HI-6121, this pin controls the byte order of transferred 16-bit data following the SPI command. When BENDI is low, "little endian" is chosen; the low order byte (bits 7:0) is transacted on the SPI before the high order byte (bits 15:8). When BENDI is high, "big endian" is chosen and the high order byte is transacted on the SPI before the low order byte.
ACKHW*	INPUT	Hardware Interrupt Acknowledge, active high. Internal 50kΩ pull-down resistor. This input is only used when the INTSEL bit in Configuration Register 1 is asserted to enable level interrupts. After interrupt assertion causes the $\overline{INTHW}$ output to go low, a high state (60ns minimum duration) on ACKHW will clear the $\overline{INTHW}$ output to logic 1. The interrupt is also cleared automatically by reading the Pending Interrupt Register.
ACKMES*	INPUT	Message Interrupt Acknowledge, active high. Internal 50kΩ pull-down resistor. This input is only used when the INTSEL bit in Configuration Register 1 is asserted to enable level interrupts. After interrupt assertion causes the $\overline{INTMES}$ output to go low, a high state (60ns minimum duration) on ACKMES will clear the $\overline{INTMES}$ output to logic 1. The interrupt is also cleared automatically by reading the Pending Interrupt Register.

*** Note:** These pins are combined into the ACKINT pin on HI-6121PQx variant.

Table 2. Pin Descriptions (HI-6120 only)

Pin	Function	Description
D15:0	I/O	Tri-state data bus for host read/write operations upon registers and shared RAM. Internal 50kΩ pull-down resistors. All read/write operations transact 16 bit words, but bus width can be configured for 8 or 16 bits. For 8 bit bus width, pins D15:8 are not connected; each 16-bit word is transacted as a pair of upper and lower byte operations, with data presented sequentially on pins D7:0. For compatibility with different host processors, the BENDI input determines whether the low order byte is transferred before the high order byte, or vice versa. See Table 4.
A15:1 and A0 / ($\overline{LB}$)	INPUTS	Address bus for host read/write operations upon registers and shared RAM. When using 16-bit bus width, address bit A0 / ($\overline{LB}$) from the host is not used. For 8-bit bus width, A0 is used to indicate which byte of the 16-bit word is currently being transferred (MSB or LSB). The logic sense of A0 is controlled by the BENDI input (see BENDI pin description and Table 4 below).
BWID	INPUT	Configuration pin for host bus width. Internal 50kΩ pull-up resistor. High selects 16-bit bus width, low selects 8-bit bus width.

Pin	Function	Description
BTYPE	INPUT	Configuration pin for host bus read/write control signal style. Internal 50kΩ pull-up resistor. High selects “Intel style” using separate read strobe $\overline{OE}$ (output enable) and write strobe $\overline{WE}$. Low selects “Motorola style” using combined read/write strobe $\overline{STR}$ and read/write select signal, R/$\overline{W}$.
R/$\overline{W}$ or $\overline{WE}$	INPUT	R/$\overline{W}$ (read/write) signal when BTYPE pin is low, or $\overline{WE}$ (write enable) when BTYPE pin is high. Internal 50kΩ pull-up resistor. Used for host read or write accesses to device RAM or registers. Important: This pin or the $\overline{CE}$ pin should be high during all address transitions.
$\overline{STR}$ or $\overline{OE}$	INPUT	When BTYPE pin is low, common $\overline{STR}$ (read/write strobe). When BTYPE pin is high, $\overline{OE}$ (output enable). Internal 50kΩ pull-up resistor. Used for host read or write accesses to device RAM or registers.
WAIT or $\overline{WAIT}$	OUTPUT	Host bus read cycle “wait” output. For compatibility with different host processors, this output can be made active high or active low, set by the state of the WPOL input pin. The WAIT output may be ignored when the host processor’s read cycle time is sufficiently slow to meet worst case (slowest) read cycle timing for this device, or when wait cycles have been enabled from the processor. The WAIT output is useful when the host processor runs at high clock rates and/or when processor read wait states do not provide adequate timing margin for worst case (slowest) read cycle timing for this device. See Section 15.1 on page 110 for further information.
WPOL	INPUT	Configuration pin for WAIT output polarity. Internal 50kΩ pull-up resistor. When WPOL is low, the “wait” output is active low ($\overline{WAIT}$). When WPOL is high, the “wait” output is active high (WAIT). The HI-6120 uses pre-fetching to speed up any series of reads from successive addresses. As long as successive reads are sequential, only the first word’s read cycle generates a WAIT ($\overline{WAIT}$) output. No WAIT is generated for following words read.

Table 3. Pin Descriptions (HI-6121 only)

Pin	Function	Description
SO	OUTPUT	Serial Peripheral Interface (SPI) Serial Output pin. SO is normally connected to MISO (Master In - Slave Out) pin on host SPI port. The SO pin is tri-stated when not transmitting serial data to host.
SI	INPUT	Serial Peripheral Interface (SPI) Serial Input pin. Internal 50kΩ pull-down resistor. SI is normally connected to MOSI (Master Out - Slave In) pin on host SPI port.
SCK	INPUT	Serial Peripheral Interface (SPI) Serial Clock pin. Internal 50kΩ pull-down resistor. SCK is normally connected to SCK output pin on host SPI port.
ACKINT (HI-6121PQX variant only)	INPUT	Interrupt Acknowledge, active high. Internal 50kΩ pull-down resistor. This input is only used when the INTSEL bit in Configuration Register 1 is asserted to enable level interrupts. After interrupt assertion causes the $\overline{INTHW}$ or $\overline{INTMES}$ output to go low, a high state (60ns minimum duration) on ACKINT will clear the $\overline{INTHW}$ or $\overline{INTMES}$ output to logic 1. Interrupt outputs on $\overline{INTHW}$ and $\overline{INTMES}$ are also cleared by reading the Pending Interrupt Register.

Table 4. HI-6120 BENDI Pin Functionality

The BENDI and A0 pins are used as outlined below to set the order for byte accesses when HI-6120 transacts 16-bit words on 16-bit or 8-bit host busses.

BENDI	BWID	A0	RD/WR	
			Host Data Bus	HI-6120 internal RAM or Register 16-bit Word
0	0	0	D[7:0]	D[7:0]
0	0	1	D[7:0]	D[15:8]
0	1	X	D[15:0]	D[7:0], D[15:8]
1	0	0	D[7:0]	D[15:8]
1	0	1	D[7:0]	D[7:0]
1	1	X	D[15:0]	D[15:8], D[7:0]

3. FUNCTIONAL OVERVIEW

The Holt HI-6120 or HI-6121 provides a complete Remote Terminal (RT) interface between a host and a MIL-STD-1553B dual redundant data bus. It automatically handles all aspects of the MIL-STD-1553 protocol, namely, encoding/decoding, message formatting, error checking, message data buffering, protocol checking, illegalization and default terminal responses. Internal static RAM is shared by the host and device logic, providing efficient storage for message data and information about messages, updated after each message transaction. The shared RAM also contains host-initialized tables that define terminal operation.

Two options are offered for host interface. The HI-6120 uses a 16-bit tri-state data bus, ideally suited for memory-mapped host processor operation. The HI-6121 uses a 3-wire Serial Peripheral Interface (SPI) with powerful SPI command set.

Figure 2 shows address mapping for registers and RAM. Registers occupy the lowest 32 addresses of the 32K memory address space. Internal registers (or contained bit fields) are partitioned as read-only or read-write so the host can exercise configuration control without risk of misconfiguration caused by accidental writes to device-maintained registers or bit fields.

Dedicated output pins convey status to the host, and generate host interrupts for preselected events. Before processing messages, internal registers and transmit data buffers in shared RAM must be initialized by the host to define the desired message responses. Host initialization can be replaced by optional auto-initialization using parameters in external EEPROM.

3.1. Shared RAM Utilization

3.1.1. Descriptor Table

The host-initialized Descriptor Table, residing in shared RAM, defines terminal response to valid commands. The table is comprised of 4-word Descriptor Blocks. Each of 32 subaddresses and 32 mode code values has two descriptor blocks, one for transmit and one for receive, for a total of 128 descriptor blocks. The first word in each descriptor block defines message options (interrupt selections, data buffer mode, etc.). Except for Indexed buffer mode (where one word counts messages) the remaining three words point to allocated data storage in shared RAM. After Master Reset is negated and before message processing, the host must initialize descriptor blocks for each utilized subaddress and mode code. Unused subaddresses and unimplemented mode codes may be illegalized (see below). The Descriptor Table Base Address Register is initialized with the starting address of the Descriptor Table. Multiple Descriptor Tables can be used for fast context switching, with the active table designated by the base address register.

3.1.2. Illegalization Table

Optional illegal command detection utilizes an Illegalization Table in the shared RAM. The table can illegalize any logical combination of 11 command word bits for subaddress, T/$\overline{R}$ bit and word count (or mode code), plus broadcast vs non-broadcast status, resulting in a total of 4,096 possible combinations. The Illegalization Table Base Address Register is initialized with the table's start address. Terminal response to an illegal command sets "message error" status and transmits Status Word only. If illegal command detection is not used (that is, no "illegal" entries in Illegalization Table), the terminal responds "in form" to all valid commands.

3.1.3. Message Data Buffers

After master reset, all locations in shared memory are reset to 0000 hex. Ordinary transmit or receive commands transfer 1 to 32 data words. These are called "subaddress commands," distinguishing them from "mode code commands," described in the next paragraph. By initializing the Descriptor Table, the host allocates space in shared RAM for storing message data words and message information words. Data pointers in the table assign separate data buffer addresses in memory for each command. Data storage arrangement differs by choice of data buffer method. Two examples are shown for each of the four buffer modes in Figures 11-18. After successfully transacting a message with one or more received data words, the RT writes into the assigned data buffer. While transacting a message with one or more transmitted data words, the RT reads data for transmission from the assigned data buffer. Before transmit commands occur, the host should write desired data into assigned transmit data buffers in shared RAM. Transmit subaddress data buffers can be optionally loaded by auto-initialization.

3.1.4. Storage for Mode Code Commands

MIL-STD-1553 defines "mode code commands" that are used for command and control, instead of data transfer. The various "mode commands" transfer a single data word, or no data word at all. The user has two choices for storing mode command data: (1) similar to subaddress command data, mode command data can be stored in RAM data buffers assigned by the host-initialized Descriptor Table, or (2) When "simplified mode command processing" is chosen, mode command data is stored

within the Descriptor Table itself. Just six defined mode commands transfer a data word; thus, option 2 is often preferred since initialization is easier. Consistent, predictable terminal responses can be set up for all mode commands, including the reserved and undefined mode codes. An option bit in Configuration Register 1 globally sets whether the 22 undefined mode commands are treated as illegal (RT response dependent on command's Illegalization Table setting) or invalid (no RT response whatsoever, and no RT status change).

3.1.5. Interrupt Log

The device maintains information from the last 16 interrupts in a 32-word circular buffer in shared RAM known as the Interrupt Log. Two 16-bit words characterize each interrupt; one word identifies the interrupt type (Interrupt Identification Word) and one word identifies the command that generated the interrupt (Interrupt Address Word). After reset, the Interrupt Log Address Register is reset to the fixed starting address of the 32 word Interrupt Log. After each occurring interrupt, the device updates the register to point to the log address used for the next occurring interrupt.

3.2. Hardware Feature Summary

3.2.1. Clock Interrupts

A 50 MHz master clock input is required. The Time-Tag counter clock is selected from six internally generated frequencies, or may use an external clock input signal.

3.2.2. Remote Terminal Address Inputs

The 5-bit Remote Terminal address is set using pins RTA0 to RTA4. The RTAP input pin should be set or reset to present matching odd parity. The state of the RT address and parity pins is latched into the Operational Status register upon rising edge on the $\overline{MR}$ master reset input. The state of the LOCK input is latched into the Operational Status register at the same time, and controls whether or not the active terminal address and parity in the Operational Status register can be overwritten by host writes into the register. Between Master Reset assertions, the state of the RTA and RTAP inputs is "don't care". If the value of RT address and parity in the Operational Status register has parity error, terminal operation is disallowed.

3.2.3. Integral Time-Tag Counter

A free-running 16-bit counter provides time-tag values that are recorded for each message transacted. The time-tag counter can be clocked from one of six internally generated frequencies, or from an external source. The user can enable automatic counter synchronization in response to "synchronize" mode commands, and optional host interrupts are provided for time-tag counter roll-over, and counter match to a stored value in the Time-Tag Utility register.

3.2.4. Dual Bus Transceivers

Built-in bus transceivers provide direct interface between the device and MIL-STD-1553 bus isolation transformers. The transceivers convert digital data to and from differential Manchester II encoded bus signals. A pair of "transmit inhibit" input pins exercises direct control over transmission for both buses.

3.2.5. Encoder and Decoders

The RT contains separate Manchester II encoders and decoders for each bus. Encoder-decoder logic interfaces directly with the dual-bus MIL-STD-1553 transceivers. The decoder checks for proper sync pulse and Manchester waveform, edge skew, correct number of bits and parity. During transmission, each encoded word is looped back through the decoder to check for errors. Bus sampling is clocked at 25 MHz, providing superior tolerance to zero-crossing distortion.

3.2.6. Auto-Initialization Serial EEPROM Interface

The device has an automatic self-initialization feature. If self-initialization is enabled after $\overline{MR}$ master reset, the device reads configuration settings from external serial EEPROM to load the Descriptor Table, Illegalization Table, transmit mode command data and registers for terminal operation. Self-initialization can optionally initialize transmit data buffers with fixed data from EEPROM. A mechanism is provided to initially program or later modify the external serial EEPROM memory, by copying host-loaded tables and register values to the serial EEPROM.

4. MEMORY AND REGISTER ADDRESSING

The HI-6120 and HI-6121 have an internal address space of 32K 16-bit words. All memory addresses in this data sheet are expressed as hexadecimal numbers, using the C programming convention where the prefix “0x” denotes a hexadecimal value; e.g., 0x00FF represents 00FF hex.

All device RAM and register address mapping is word oriented, rather than byte oriented. Register and memory addresses throughout this document reflect word addressing. For all HI-6121 and most HI-6120 applications, word oriented addressing applies. Word oriented addressing with the HI-6120 uses address inputs A15 to A1; address input A0 is not used as fifteen bits are sufficient for a 32K address range.

HI-6120 ONLY: When required by the application, the host bus interface HI-6120 is able to use byte transfers. All 8-bit microprocessors (and some 16-bit and 32-bit microprocessors) use (or can use) byte-oriented memory accesses. To provide byte capability, the HI-6120 has a sixteenth bus address input, A0. Byte oriented addressing with the HI-6120 uses all 16 address pins, A15:A0 to address 64K bytes. The A0 input denotes whether the first or second byte in the word is being addressed, while A15:A1 indicate the word address. This difference must be considered when assigning HI-6120 pointer values or accessing RAM or registers. From the microprocessor’s standpoint, any host-assigned RAM buffer address will be double the value of the buffer’s pointer stored in RAM. **This paragraph only applies to HI-6120 using 8-bit bus width.** From this point on, all register and memory addresses presented in this data sheet are 15-bit word addresses.

From the host standpoint, register operations and RAM operations are performed identically. Registers occupy the lowest 32 addresses, 0x0 to 0x001F. Depending on function, individual registers may be read-only, read-write, or a combination of read-only and read-write bit fields. Read-only registers, and read-only bit fields contained in registers, are protected against accidental host overwrite by device logic.

Addresses in the range 0x0020 to 0x7FFF apply to static RAM memory. All RAM is read-write and can be written or read by either the host or the internal device logic.

Some memory locations (specifically Descriptor Table Control Words) contain bits updated by both host and device. These locations are protected against accidental data collision by device arbitration logic which acts when concurrent writes by both host and device occur.

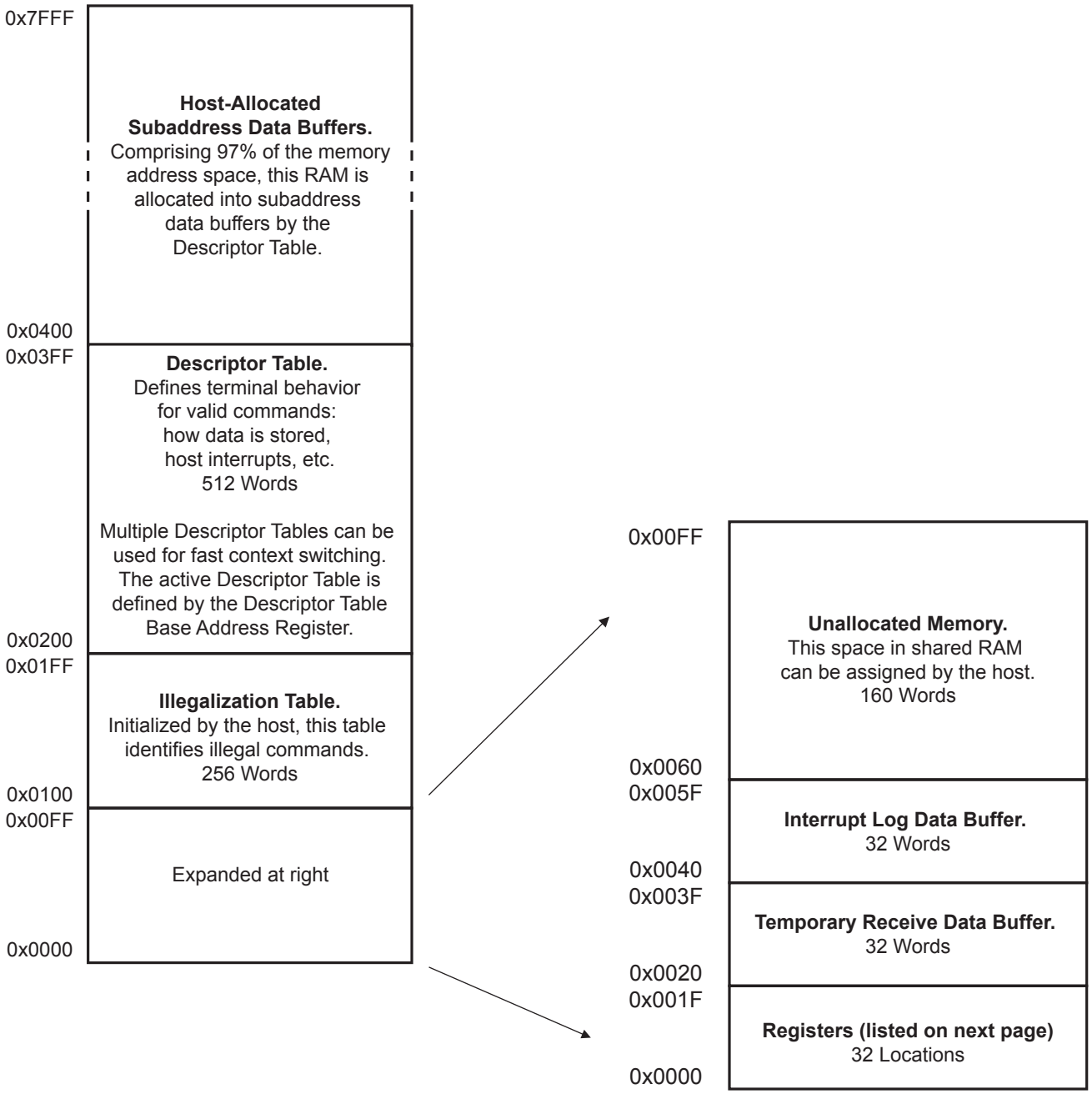


Figure 2. Address Mapping for Registers and RAM

5. REGISTERS

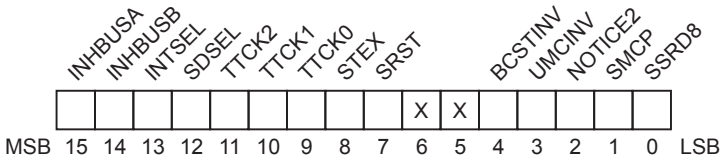
Residing at the start of the memory address space, 32 addresses are reserved for HI-6120 and HI-6121 registers. Register addresses overlay the shared RAM address space, but are separate from the shared dual-port RAM. All register bits are active high. Unless otherwise indicated, all registers are reset in software to the logic zero condition after Master Reset (except any bits reflecting the state of input pins). For all registers, bit 15 is the most significant.

Table 5. Register Summary

Register Number	*Hex Address*	*Register Name*
0	0x0000	Configuration Register 1
1	0x0001	Configuration Register 2
2	0x0002	Operational Status Register
3	0x0003	Current Command Register
4	0x0004	Current Control Word Address Register
5	0x0005	Descriptor Table Base Address Register
6	0x0006	Pending Interrupt Register
7	0x0007	1553 Status Word Bits Register
8	0x0008	Time-Tag Register
9	0x0009	Interrupt Log Address Register
10	0x000A	Current Message Information Word Address Register
11-14	0x000B-0x000E	Reserved
15	0x000F	Memory Address Pointer (HI-6121 Only)
16	0x0010	Interrupt Enable Register
17	0x0011	Time-Tag Utility Register
18	0x0012	Bus A Select Register
19	0x0013	Bus B Select Register
20	0x0014	Built-In Test (BIT) Word Register
21	0x0015	Alternate Built-In Test (BIT) Word Register
22	0x0016	Reserved
23	0x0017	Test Control Register
24	0x0018	Loopback Test Transmit Data Register
25	0x0019	Loopback Test Receive Data Register
26-31	0x001A-0x001F	Reserved

5.1. Configuration Register 1 (0x0000)

This 16-bit register is Read-Write and is fully maintained by the host. All bits are active high.



NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

When configuring registers and RAM following Reset, "Configuration Register 1 (0x0000)" should always be written **last** to ensure configuration and initialization is complete **before** starting terminal operation (i.e. this ensures STEX bit is not set until after configuration is complete). See "14.1. Master Reset using the MR pin and Optional Auto-Initialization" for further details.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	INHBUSA	R/W	0	Bus A Inhibit. When set, this bit disables transmit and receive for Bus A. This bit is logically ORed with the TXINHA input signal to control Bus A transmitter enablement. Bus A transmission is disabled if the INHBUSA register bit or TXINHA input pin is asserted. The TXINHA pin does not affect the Bus A receiver.
14	INHBUSB	R/W	0	Bus B Inhibit. When set, this bit disables transmit and receive for Bus B. This bit is logically ORed with the TXINHB input signal to control Bus B transmitter enablement. Bus B transmission is disabled if the INHBUSB register bit or TXINHB input pin is asserted. The TXINHB pin does not affect the Bus B receiver.
13	INTSEL	R/W	0	Interrupt Mode Select. When this bit is low, pulse interrupt outputs are selected for $\overline{INTMES}$ and $\overline{INTHW}$ output pins. When this bit is high, level interrupts are enabled which require host acknowledgment for interrupt pin reset.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>12</td><td>SDSEL</td><td>R/W</td><td>0</td><td>Shutdown Select.

This bit affects terminal response to “transmitter shutdown” mode code commands and only applies when the MCOPT4 bit in Configuration Register 2 equals logic 0 for automatic shutdown after “transmitter shutdown” and “selected transmitter shutdown” mode code commands. When MCOPT4 and SDSEL are both logic 0, a valid “transmitter shutdown” mode command automatically disables the inactive bus transmitter and receiver (complete ”bus shutdown”). This is the recommended mode of operation and is the default state of these two bits after $\overline{MR}$ reset.

When MCOPT4 is logic 0 and SDSEL is logic 1, “transmitter shutdown” or “selected transmitter shutdown” mode commands automatically disable just the inactive bus transmitter, but the bus receiver remains enabled. The terminal fully complies with valid commands received on the inactive bus (storing received data, etc.), except it does not transmit status or data onto that bus (”mute terminal”). This mode of operation is not recommended but may be required in some applications. See MCOPT4 bit in Configuration Register 2 for further information concerning “transmitter shutdown” and “selected transmitter shutdown” mode commands. The Built-In Test (BIT) Word Register contains status flags that reflect automatic shutdown status when the MCOPT4 bit in Configuration Register 2 is logic 0. **See page xx.**</td></tr>
<tr><td>11, 10, 9</td><td>TTCK2:0</td><td>R/W</td><td>0</td><td>Time-Tag Counter Clock Select. These three bits select the time-tag counter clock source from the following options:

<table>
<tr><th>TTCK2</th><th>TTCK1</th><th>TTCK0</th><th>Clock Source</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Time-Tag counter disabled</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>External clock provided at TTCK input pin</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Internally generated 2µs clock</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internally generated 4µs clock</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Internally generated 8µs clock</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Internally generated 16µs clock</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Internally generated 32µs clock</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Internally generated 64µs clock</td></tr>
</table></td></tr>
<tr><td>8</td><td>STEX</td><td>R/W</td><td>0</td><td>Start Execution.

Assertion of this bit initiates RT operation; negation of this bit inhibits or stops RT operation. Upon STEX assertion, RT parity-address error prevents terminal operation, regardless of the logical state of the STEX bit. If RT address parity error occurs, the Status Register and Pending Interrupt Register RTAPF bits will be asserted. This bit is cleared after $\overline{MR}$ pin master reset.</td></tr>
<tr><td>7</td><td>SRST</td><td>R/W</td><td>0
(SR = 0)</td><td>Software Reset.

Assertion of this bit immediately initiates the software reset process. This bit should not be set to logic 1 during auto-initialization. This bit is cleared after $\overline{MR}$ master reset and automatically self-resets after being set by the host.</td></tr>
<tr><td>6,5</td><td>-----</td><td>R/W</td><td>0
(SR = 0)</td><td>Not used.</td></tr>
</table>

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
4	BCSTINV	R/W	0	Broadcast Commands Invalid. If this bit is high, commands addressed to RT address 31 are treated as invalid: There is no terminal recognition of commands to RT address 31; there is no RT command response, and no status updating for the benefit of following “transmit status” or “transmit last command” mode commands. If this bit is low, commands addressed to RT address 31 are treated as valid broadcast commands.
3	UMCINV	R/W	0	Undefined Mode Codes Invalid. This bit globally defines whether undefined mode code commands are treated as valid (default) or invalid commands. This bit applies only to the following undefined mode code commands: Mode Codes 0 through 15 with T/$\overline{R}$ bit = 0 Mode Codes16, 18 and19 withT/$\overline{R}$ bit = 0 Mode Codes 17, 20 and 21 with T/$\overline{R}$ bit = 1 If this bit is low (default state after $\overline{MR}$ pin reset) undefined mode code commands are considered valid, and RT response is based on individual mode command settings in the Illegalization Table: If a mode command is legal, the RT “responds in form” and updates status. If a mode command is illegal, the RT asserts Message Error status and (if non-broadcast) transmits only its Status Word without associated data word. Later in this data sheet, the section “RT Message Responses, Options & Exceptions” fully describes terminal response for each mode code value, command word T/$\overline{R}$ bit state, and option settings. If this bit is high, undefined mode code commands are treated as invalid: There is no RT recognition of an invalid command, no RT command response, and no status updating for the benefit of following “transmit status” or “transmit last command” mode commands.
2	NOTICE2	R/W	0	If this bit is high, the terminal stores data associated with broadcast commands separately from data associated with non-broadcast commands to meet the requirements of MIL-STD-1553B Notice 2. If this bit is low, broadcast command data is stored in the same buffer as non-broadcast command data.
1	SMCP	R/W	0	Simplified Mode Command Processing. When asserted, the device applies simplified processing for all valid mode code commands. The later section entitled “Mode Command Processing” describes this option.
0	SSRD8	R/W	0	Single-Strobe Read for 8-Bit Parallel Bus Mode. This bit only applies to HI-6120 (not HI-6121) and only applies when the parallel host bus is configured for 8-bit bus width. When performing 2-byte read accesses of external memory, some microprocessors with 8-bit bus assert individual Read Enable (or $\overline{STROBE}$) pulses for high and low bytes. Other microprocessors assert a single, wider Read Enable (or $\overline{STROBE}$) pulse, while simply changing the low address bit (A0 / $\overline{LB}$) to access the two bytes. For this last case, the SSRD8 bit should be set when writing device configuration, before register or RAM readback is performed.

5.2. Configuration Register 2 (0x0001)

This 16-bit register is Read-Write and is fully maintained by the host. All bits are active high.

NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). This register is unaffected by software reset.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15,14	TOSEL1:0	R/W	0	Time-Out Select for RT-RT Receive Commands. These bits select the "no response" time-out for RT-RT receive commands. Message error occurs when the transmitting Remote Terminal fails to begin transmission before time-out occurs. Time interval boundaries are defined in RT validation test plan Figure 8 "RT-RT Timeout Measurement." MIL-STD-1553B stipulates that 54 to 60µs is the acceptable range for time-out. However, longer time-out options are provided for systems using long buses and/or utilizing bus repeaters that add delay to bus traffic. RT-RT time-out can be selected from the following options:
				TOSEL1: 1, 1, 0, 0 — TOSEL0: 1, 0, 1, 0 — RT-RT Time-Out: 150µs, 125µs, 100µs, 57µs (default after $\overline{MR}$ pin master reset)
13	TRXDB	R/W	0	Temporary Receive Data Buffer. Setting this bit enables a temporary data buffer for all receive commands. When enabled, the RT stores received data words in a 32-word data buffer during message processing. Upon error-free message completion, all saved words are written to data buffer memory in a burst. When the temporary receive data buffer is disabled, the RT writes each received data word to the subaddress data buffer memory as it is received. Should message error occur during data word reception, this mode results in loss of data integrity, as vaild data from the prior command is partially overwritten by data from a message with error. MIL-STD-1553 states that data should be disregarded for messages ending in error. This bit should only be modified while Configuration Register 1 STEX bit is low. Changes occurring while STEX = 1 cause unpredictable results. In a typical application, the buffer is not directly accessed by the host, although there is no restriction preventing host data access.
12	TTLOAD	R/W	0	Load Time-Tag Counter. When this bit is written from logic 0 to logic 1, data contained in the Time-Tag Utility register is written to the Time-Tag counter. The TTLOAD register bit self-resets after use. See MCOPT3 bit which affects automatic Time-Tag counter loading upon "synchronize" mode command with data word.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
11	RTTAG	R/W	0	Reset Time-Tag Counter. Assertion of this bit clears the Time-Tag counter and counting is disabled until the bit is negated. Also the “synchronize” mode command (MC1) causes automatic Time-Tag counter reset.
10	ALTBITW	R/W	0	Alternate BIT Word Enable. If this bit is logic 0, the device responds to a “transmit BIT word” mode command (MC19) by sending the word stored in the Built-In Test Word register, at address 0x0014. If this bit is logic 1, the terminal transmits the word stored in the Alternate Built-In Test Word register, at address 0x0015. The alternate register allows the user to fully define the BIT word, while the default register location contains several predefined, device-controlled status bits.
9	MCOPT4	R/W	0	Mode Code Option 4. ***Note:*** *Mode commands MC4 and MC5 are not affected by the MCOPT4 bit, but are included in this description to present a complete picture of device response to bus shutdown mode commands.* The Bus Controller exercises “shutdown“ control over the terminal’s connection to the inactive MIL-STD-1553 bus using the “transmitter shutdown” (MC4) or “selected transmitter shutdown” (MC20 decimal) mode code commands. When the inactive transmitter is shutdown, the HI-612x device inhibits further transmission on that bus. Once shutdown, the transmitter can be reactivated by (a) an “override transmitter shutdown” (MC5) mode command, (b) an “override selected transmitter shutdown” (MC21 decimal) mode command, (c) a “reset remote terminal” (MC8) mode command, (d) hardware $\overline{MR}$ master reset or (e) software reset by setting the SRST bit in Configuration Register 1. When the MCOPT4 bit is reset, the device automatically performs bus shutdown and shutdown override in response to mode commands. When the MCOPT4 bit is set, the device only transmits status; the host must perform bus shutdown and override duties by asserting control of the TXINHA and TXINHB bits in Configuration Register 1, or by controlling the input pins with the same function. Mode commands MC4 (”transmitter shutdown”) and MC5 (”override transmitter shutdown”) have unconditional shutdown or override response. When MC4 is received, the terminal fulfills shutdown for the inactive bus, disabling the transmitter and receiver, or transmitter only, depending on the state of the SDSEL bit in Configuration Register 1. The device affirms shutdown status by updating bits 15-12 in the BIT Word Register. When mode command MC5 is received, inactive bus transmit and receive is automatically reenabled by the device; “shutdown override” status is affirmed by resetting the inactive bus shutdown bit(s) in the BIT Word Register.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="6">9</td><td rowspan="6">MCOPT4
(continued)</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td>The “selected transmitter shutdown” (MC20 decimal) and “override selected transmitter shutdown” (MC21 decimal) mode commands act similarly to MC4 and MC5 respectively, except bus shutdown (or shutdown override) is conditional, based on the value of a mode data word received with the command. To act on a given bus, the received mode data word must match a predetermined “bus select” value. Bus shutdown (or shutdown override) can only act on the inactive bus, and only when the received mode data word matches the “bus select” value for that bus. When a MC20 mode data word matches the “bus select” value for the inactive bus, the terminal fulfills shutdown for the inactive bus, disabling the transmitter and receiver, or transmitter only, depending on the state of the SDSEL bit in Configuration Register 1. The device affirms shutdown status by updating bits 15-12 in the BIT Word Register. When a MC21 mode data word matches the “bus select” value for the inactive bus, the terminal fulfills shutdown override for the inactive bus, enabling the transmitter (and receiver, if the SDSEL bit in Configuration Register 1 is logic 0). The device affirms override status by resetting bits 15-12 in the BIT Word Register.

When the MCOPT4 bit equals zero, unique “bus select” values should be initialized by the host in the “Bus A Select” register (0x0012) and “Bus B Select” register (0x0013) for fulfillment of “selected transmitter” shutdown and override mode commands. When MCOPT4 equals zero, transmitter shutdown (or shutdown override) automatically occurs when the received mode data value matches the inactive bus “Bus Select” register.

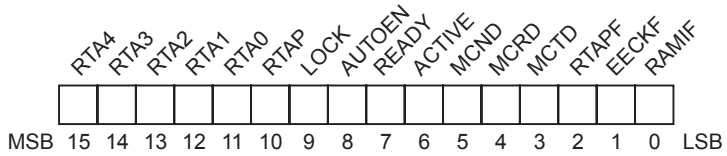
Below shows device response for “transmitter shutdown” and “override transmitter shutdown” mode code commands for different option configurations:</td></tr>
<tr><td>The MCOPT4 bit in Configuration Register 2 is logic 0 or 1</td></tr>
<tr><td>
<table>
<tr><td>MC4 (or MC5)
unconditional fulfillment</td><td>Inactive Bus Tx & Rx Disabled (Enabled).
(only Tx is disabled, if the SDSEL config. bit = 1)</td><td>Status Word transmitted, unless broadcast</td><td>In BIT Word Register, TXSD & RXSD bits updated.
(only TXSD bit updated, if the SDSEL config. bit = 1)</td></tr>
</table>
</td></tr>
<tr><td>The MCOPT4 bit in Configuration Register 2 is logic 0</td></tr>
<tr><td>
<table>
<tr><td>MC20 (or MC21)
if mode data value matches “Bus Select” value</td><td>Inactive Bus Tx & Rx Disabled (Enabled).
(only Tx is disabled, if the SDSEL config. bit = 1)</td><td>Status Word transmitted, unless broadcast</td><td>In BIT Word Register, TXSD & RXSD bits updated.
(only TXSD bit updated, if the SDSEL config. bit = 1)</td></tr>
<tr><td>MC20 (or MC21)
if mode data does NOT match “Bus Select” value</td><td>Inactive Bus Tx & Rx status not changed</td><td>Status Word transmitted, unless broadcast</td><td>In BIT Word Register, TXSD & RXSD bits are static</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="3">9</td><td rowspan="3">MCOPT4 (continued)</td><td rowspan="3">R/W</td><td rowspan="3">0</td><td colspan="4">The MCOPT4 bit in Configuration Register 2 is logic 1</td></tr>
<tr><td>MC20 (or MC21) if mode data value matches “Bus Select” value</td><td>Inactive Bus Tx & Rx status NOT changed (Host can modify BUSINH bit in Configuration Reg 1)</td><td>Status Word transmitted, unless broadcast</td><td>In BIT Word Register, TXSD & RXSD bits are static</td></tr>
<tr><td>MC20 (or MC21) if mode data does NOT match “Bus Select” value</td><td>Inactive Bus Tx & Rx status not changed</td><td>Status Word transmitted, unless broadcast</td><td>In BIT Word Register, TXSD & RXSD bits are static</td></tr>
<tr><td>8,7</td><td>MCOPT3:2</td><td>R/W</td><td>0</td><td colspan="4">Mode Code Options 3 and 2.
If both of these bits equal one, the data word received with a valid “synchronize” mode command (MC17) is unconditionally loaded into the Time-Tag counter. For non-broadcast MC17 commands, the counter load occurs before status word transmission. If both of these bits equal 0, the external host assumes responsibility for actions needed to perform “synchronize” duties upon reception of the valid MC17 “synchronize”mode code command, but status transmission automatically occurs.
The binary 01 and 10 combinations of the MCOPT3 and MCOPT2 bits support certain extended subaddressing schemes. If the MCOPT3-MCOPT2 bits equal 01, the received data word is automatically loaded into the Time-Tag counter if bit 0 of the received data word equals 0. If the MCOPT3-MCOPT2 bits equal 10, the received data word is automatically loaded into the Time-Tag counter if bit 0 of the received data word equals 1. For non-broadcast MC17 commands, the counter load occurs before status word transmission.</td></tr>
<tr><td>6</td><td>MCOPT1</td><td>R/W</td><td>0</td><td colspan="4">Mode Code Option 1.
If this bit is logic 0, reception of a “transmit vector word” mode command (MC16) causes automatic reset of the Service Request status bit. The Service Request bit is reset in the Status Word Bits register before status word transmission begins. If the MCOPT1 bit is logic 1, the external host assumes responsibility for resetting the Service Request bit in the Status Word Bits register.</td></tr>
<tr><td>5</td><td>MCOPT0</td><td>R/W</td><td>0</td><td colspan="4">Mode Code Option 0.
If this bit is logic 0, reception of a “reset remote terminal” mode command (MC8) causes automatic assertion of SRST software reset. If non-broadcast mode command, reset occurs after status word transmission is complete. If this bit is logic 1, the external host assumes responsibility for actions needed to perform terminal reset.</td></tr>
<tr><td>4</td><td>-----</td><td>R/W</td><td>0</td><td colspan="4">Not Used</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Function
3	GPBCST	R/W	0	Message Information Word Gap Error / Broadcast Flag. When GPBCST = 0, bit 13 GAP/BCAST in Receive and Transmit "Subaddress Message Information Words" on page 71 and Receive and Transmit "Mode Command Message Information Words" on page 74 is a **Gap Error flag**. When GPBCST = 1, bit 13 GAP/BCAST in Receive and Transmit "Subaddress Message Information Words" on page 71 and Receive and Transmit "Mode Command Message Information Words" on page 74 is a **Broadcast flag**.
2	-----	R/W	0	Not Used
1	DPBTOFF	R/W	0	Disable ping pong DPB pointer toggle when the received valid command is illegal, or when a message occurs with Busy status. When DPBTOFF = 0, the DPB buffer pointer never toggles for valid, legal messages ending in error, but will toggle when the received valid command is illegal, or when a message occurs with Busy status. Setting DPBTOFF = 1 disables ping pong DPB pointer toggle when the received valid command is illegal, or when a message occurs with Busy status. Therefore, in the case with DPBTOFF = 1, the DPB bit only toggles upon completion of a message with successful data transfer. The complemented DPB bit in the Rx or Tx Control Word will always indicate the buffer holding the last-transacted "good" data. See "Ping-Pong Data Buffering" on page 79.
0	IRQOFF	R/W	0	Setting this bit will suppress $\overline{IRQ}$ interrupt pin assertion for enabled RT message interrupts if the message is illegal. Illegal messages are defined in the "Command Illegalization Table" on page 49. Note that a given Rx or Tx subaddress can contain both legal and illegal word counts. Interrupt assertion is prevented when commands are received for illegal data word counts. This option does not affect logging of message interrupts in the Interrupt Log Buffer, so the host can see when such commands were received. When an illegal message occurs, an Interrupt Identification Word (IIW) and Time Tag Word (TTW) are written into the "Interrupt Log Buffer" on page 53 (but data word locations in the buffer ARE NOT updated. The logged IIW shows Broadcast, Message Error and or Illegal Message status for such messages. The IIW matches the format of the "Pending Interrupt Register (0x0006)" on page 31.

5.3. Operational Status Register (0x0002)

All sixteen register bits are active high. After rising edge on the $\overline{MR}$ master reset input pin, bits 15 - 8 reflect the state of input pins RTA4 through RTA0, RTAP, LOCK and AUTOEN; register bits 7 - 3 are reset to logic 0 state. Register bits 8 - 0 are always read-only. If the register's LOCK bit is logic 0, bits 15 - 9 are read-write but cannot be written unless STEX in Configuration Register 1 is low. If the register LOCK bit is logic 1, bits 15 - 9 are is read-only. Once the LOCK bit is set, unlock requires a new $\overline{MR}$ master reset assertion with the LOCK input pin at logic 0 state.



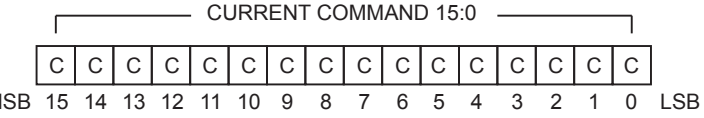
NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The value "PIN" denotes the bit is set to the value of the corresponding pin following Master Reset. This register is unaffected by software reset.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15-11	RTA4 - 0	R/W	PIN	Remote Terminal Address bits 4 - 0.
10	RTAP	R/W	PIN	Remote Terminal Address Parity. These bits contain the active remote terminal address. After a rising edge on the $\overline{MR}$ master reset input signal, these bits reflect the state of the RTA4 - 0 and RTAP input pins. When the register LOCK bit is high, these bits are read-only. When the register LOCK bit is low (and STEX in Configuration Register 1 equals 0) auto-initialization (see bit 8) or the host can overwrite these bits to change the terminal address and parity.
9	LOCK	R/W	PIN	Terminal Address Lock. After a rising edge on the $\overline{MR}$ master reset input signal, this bit reflects the state of the LOCK input pin. When the LOCK bit is high, this bit is read-only. When LOCK is low (and STEX in Configuration Register 1 equals 0) auto-initialization (see bit 8) or the host can write this bit to logic 1 to lock the active terminal address.
8	AUTOEN	R	PIN	Auto-Initialize Enable. This read-only bit reflects the state of the AUTOEN input pin that applied at the rising edge on the $\overline{MR}$ master reset input signal. If the register AUTOEN bit is high, device auto-initialization was performed following $\overline{MR}$ reset. When auto-initialization is complete, the device waits for the host to assert the STEX bit in Configuration Register 1 to enable terminal operation. Auto-initialization of the Control Register can optionally set STEX to begin terminal operation without host assistance. See section entitled "Reset and Initialization" for details.
7	READY	R	0	Ready status. This read-only bit reflects the state of the output pin READY and is cleared on reset. The bit is asserted after post-reset internal terminal initialization is complete, indicating that shared RAM is ready to accept configuration data from the host.
6	ACTIVE	R	0	Active status. When set, this read-only bit indicates the terminal is presently processing a message. This bit reflects the state of output pin ACTIVE and is cleared on reset. Note: Ths bit and the corresponding output pin are asserted upon valid command detection and negated when command processing is completed.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td rowspan="7">5,4,3</td><td rowspan="7">MCND
MCRD
MCTD</td><td rowspan="7">R</td><td rowspan="7">0</td><td>Mode Code Command Type Flags (No-Data, Receive-Data and Transmit-Data).
These three bits reflect the state of the command stored in the Current Command Register, 0x0003:
<table>
<tr><th>Current Command Type</th><th>MCND</th><th>MCRD</th><th>MCTD</th><th>Current Command Word</th></tr>
<tr><td>Subaddress (not mode code)</td><td>0</td><td>0</td><td>0</td><td>Subaddress, transmit or receive</td></tr>
<tr><td>Mode code (no data word)</td><td>1</td><td>0</td><td>0</td><td>MC0 to MC15, T/$\overline{R}$ bit equals 1</td></tr>
<tr><td>Mode code (receive data)</td><td>0</td><td>1</td><td>0</td><td>MC16 to MC31, T/$\overline{R}$ bit equals 0</td></tr>
<tr><td>Mode code (transmit data)</td><td>0</td><td>0</td><td>1</td><td>MC16 to MC31, T/$\overline{R}$ bit equals 1</td></tr>
<tr><td>Mode code (undefined, no data)</td><td>1</td><td>1</td><td>1</td><td>MC0 to MC15, T/$\overline{R}$ bit equals 0</td></tr>
</table></td></tr>
<tr><td>2</td><td>RTAPF</td><td>R</td><td>0</td><td>RT Address Parity Fail.
This bit is set when Remote Terminal address parity error is present. The bit is low when correct odd parity applies to the terminal address latched in bits 15-10. This bit is high when parity error is present.</td></tr>
<tr><td>1</td><td>EECKF</td><td>R</td><td>0</td><td>EEPROM Checksum Fail.
This bit only applies when auto-initialization is enabled. While performing auto-initialization, this bit is set if the checksum tallied from read EEPROM data doesn’t match the checksum value stored in EEPROM. This failure also sets bit 1 in the Built-In Test Word Register (0x0014).</td></tr>
<tr><td>0</td><td>RAMIF</td><td>R</td><td>0</td><td>RAM Initialization Fail.
This bit only applies when auto-initialization is enabled. While performing initialization, this bit is set if a write-then-read RAM value doesn’t match its counterpart location in the serial EEPROM. This failure also sets bit 1 in the Built-In Test Word Register (0x0014).</td></tr>
</table>

5.4. Current Command Register (0x0003)

This 16-bit register is Read-Only and is fully maintained by the device.

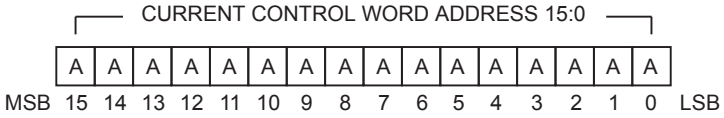


NOTE: ‘*Reset*’ refers to bit value following Master Reset ($\overline{MR}$). This register is unaffected by software reset.

Bit No.	Mnemonic	R/W	Reset	Function
15-0	CC15:0	R	0	Current Command Word. This register contains the last valid command received over either MIL-STD-1553 bus. This register is updated 5us after the ACTIVE output is asserted. Bit 15 is MSB.

5.5. Current Control Word Address Register (0x0004)

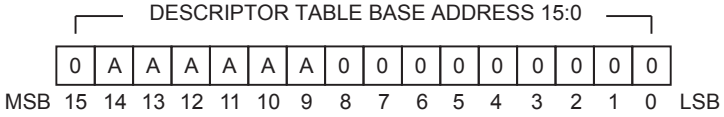
This 16-bit register is Read-Only and is fully maintained by the device.



NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). This register is unaffected by software reset.

Bit No.	Mnemonic	R/W	Reset	Function
15-0	CCW15:0	R	0	Current Control Word Address Register This register contains the address for the descriptor table Control Word corresponding to the current command stored in the Current Command Register (0x0003). This register is updated 5us after the ACTIVE output is asserted. Bit 15 is MSB. Also see "Current Message Information Word Address" register, 0x000A.

5.6. Descriptor Table Base Address Register (0x0005)

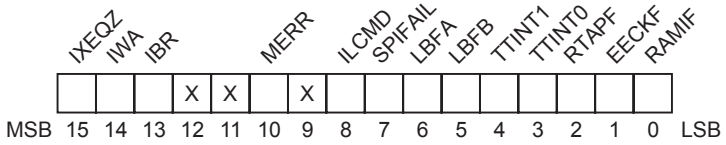


This 16-bit register is Read-Write and is fully maintained by the host. **This register is loaded with 0x0200 after $\overline{MR}$ pin master reset or SRST software reset.** The host maintains this register to specify the starting address for the Descriptor Table. For fast context switching, the host may initialize multiple Descriptor Tables, then update this register to load the new base address when the active Descriptor Table changes. The base address must be chosen with bits 7:0 = 00000000. These bits (and the highest address bit) cannot be set in the register. The primary Descriptor Table (enabled at reset) should reside at address space 0x0200 to 0x03FF. Other tables (if used) could begin at address multiples of 0x0200, like 0x0400 and 0x0600. Bit 15 and bits 8:0 cannot be set and will always read logic 0. Thus a value written by the host must equal or exceed 0x200.

5.7. Pending Interrupt Register (0x0006)

This 16-bit register is Read-Only. If the corresponding bit is set in the Interrupt Enable Register when a predetermined interrupt-causing event occurs, these actions occur: (1) a pending interrupt bit is set in this register, (2) the $\overline{INTMES}$

or $\overline{\text{INTHW}}$ output is asserted, depending on interrupt type, (3) the interrupt is registered in the Interrupt Log. If the corresponding bit is reset in the Interrupt Enable Register when a predetermined interrupt-causing event occurs, there is no reaction. To simplify host interrupt management, when the host reads this register, the Pending Interrupt Register automatically resets to 0x0000. For further information on interrupt behavior, also see descriptions for Interrupt Enable register and Interrupt Log Address register, and refer to the later section entitled “Interrupt Management”.



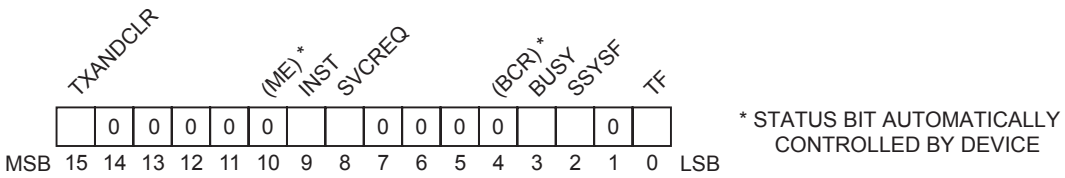
NOTE: ‘*Reset*’ refers to bit value following Master Reset ($\overline{\text{MR}}$). This register is unaffected by software reset.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	IXEQZ	R	0	Index Equal Zero Interrupt. If the IXEQZ bit is set in the Interrupt Enable register and the subaddress descriptor Control Word allows the IXEQZ interrupt, this bit is asserted for (a) subaddresses using indexed buffer mode when the index decrements from 1 to 0, or (b) subaddresses using circular buffer modes when the pre-determined number of messages has been transacted. The $\overline{\text{INTMES}}$ output is asserted and the Interrupt Log is updated.
14	IWA	R	0	Interrupt When Accessed. If the IWA bit is set in the Interrupt Enable register and the subaddress descriptor Control Word allows the IWA interrupt, this bit is asserted each time a valid legal message is transacted for the subaddress. The $\overline{\text{INTMES}}$ output is asserted and the Interrupt Log is updated.
13	IBR	R	0	Broadcast Command Received Interrupt. If the IBR bit is set in the Interrupt Enable register and the subaddress descriptor Control Word allows the IBR interrupt, this bit is asserted each time a valid legal broadcast message is transacted for the subaddress. The $\overline{\text{INTMES}}$ output is asserted and the Interrupt Log is updated.
12,11	-----	R	0	Not used.
10	MERR	R	0	Message Error Interrupt. If the MERR bit is set in the Interrupt Enable register, this bit is asserted when a message error is detected. Errors can be caused by Manchester encoding problems or protocol errors. The $\overline{\text{INTMES}}$ output is asserted and the Interrupt Log is updated.
9	-----	R	0	Not used.
8	ILCMD	R	0	Illegal Command Interrupt. If the ILCMD bit is set in the Interrupt Enable register, this bit is asserted each time an illegal message (determined by the Illegalization Table) occurs for a new command. The $\overline{\text{INTMES}}$ output is asserted and the Interrupt Log is updated. **See section “Illegalization Table” for additional information.**

Bit No.	Mnemonic	R/W	Reset	Function
7	SPIFAIL	R	0	SPI Fail Interrupt (HI-6121 only). The HI-6121 uses a SPI interface for host access. The device operates in SPI Slave mode. If the SPIFAIL bit is set in the Interrupt Enable register, this bit is asserted each time an incorrect number of SCK clocks occurs during SPI chip select assertion, The $\overline{\text{INTHW}}$ output is asserted and the Interrupt Log is updated.
6,5	LBFA, LBFB	R	0	Loopback Fail Bus A and Loopback Fail Bus B Interrupts. During all transmitted command responses, the device compares words transmitted to the received and decoded words detected on the bus. If the LBFA or LBFB bit is set in the Interrupt Enable register, this bit is asserted each time this loopback detects mismatch. The $\overline{\text{INTMES}}$ output is asserted and the Interrupt Log is updated.
4	TTINT1	R	0	Time-Tag Interrupt 1. If the TTINT1 bit is set in the Interrupt Enable register, this bit is asserted each time the free-running Time-Tag counter value matches the value stored in the Time-Tag Utility Register. The $\overline{\text{INTHW}}$ output is asserted and the Interrupt Log is updated.
3	TTINT0	R	0	Time-Tag Interrupt 0. If the TTINT0 bit is set in the Interrupt Enable register, this bit is asserted each time the free-running Time-Tag counter value rolls over from full count 0xFFFF to 0x0000. The $\overline{\text{INTHW}}$ output is asserted and the Interrupt Log is updated.
2	RTAPF	R	0	RT Address Parity Fail Interrupt. This bit is asserted when RT address and parity bits latched in the Operational Status Register do not exhibit odd parity (odd number of bits having logic 1 state). Because the RTAPF bit is always set in the Interrupt Enable register, the $\overline{\text{INTHW}}$ output is asserted and the Interrupt Log is updated. When parity error occurs, the RT will not begin operation, regardless of the state of the Control Register STEX bit.
1	EECKF	R	0	Initialization EEPROM Checksum Fail Interrupt. This bit is asserted if serial EEPROM checksum failure occurs during auto-initialization. Because the EECKF bit is always set in the Interrupt Enable register, the $\overline{\text{INTHW}}$ output is asserted and the Interrupt Log is updated.
0	RAMIF	R	0	RAM Initialization Fail Interrupt. This bit is asserted after auto-initialization if an initialized RAM location does not match its 2 corresponding serial EEPROM locations. Because the RAMIF bit is always set in the Interrupt Enable register, the $\overline{\text{INTHW}}$ output is asserted and the Interrupt Log is updated.

5.8. 1553 Status Word Bits Register (0x0007)

This 16-bit register is Read-Write and is fully maintained by the host. All bits are active high. Bits set in this register are reflected in the outgoing MIL-STD-1553 status word.



The"dynamic bus control acceptance" bit is not implemented; this device cannot function as bus controller. The host controls the Instrumentation, Busy, Terminal Flag, Service Request and Subsystem Flag status word bits by writing to bits 9:0 in this register. Remote terminal status word responses reflects the assertion of these register bits until negated by the host, unless the Immediate Clear function (bit 15) is enabled. The position of register bits 4 and 10 correspond to the Broadcast Command Received (BCR) and Message Error (ME) bits in the terminal status word. Transmit state for the BCR and ME bits in the terminal's status word is controlled by the device, based on prior command transactions. This pair of register bits cannot be set by a host write operation and always read back logic 0, so do not reflect the true status of these status flags.

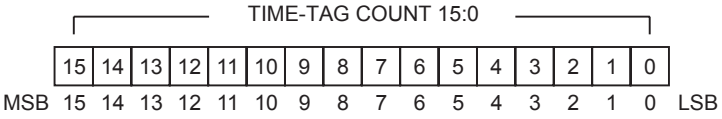
NOTE: '*Reset*' refers to bit value following either Master Reset ($\overline{MR}$) or software reset.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	TXANDCLR	R/W	0	Transmit (Once) and Clear. When this bit is set, the register is cleared after any set bits 0-9 are used once in a transmitted status word. This bit does not affect operation of the Transmit Status Word and Transmit Last Command mode codes. Example: Transaction of a valid legal command with the INST and TXANDCLR bits asserted results in status word transmission with the Instrumentation bit set. If the following command is Transmit Status or Transmit Last Command mode code, the Instrumentation bit remains set.
14-10	-----	R	0	Not used, these bits cannot be set.
9	INST	R/W	0	Instrumentation. When this bit is asserted, the Instrumentation status bit is set.
8	SVCREQ	R/W	0	Service Request. When this bit is asserted, the Service Request status bit is set.
7-4	-----	R	0	Not used, these bits cannot be set.
3	BUSY	R/W	0	Busy (global). When this bit is asserted, the device asserts Busy bit in status response for all valid commands. Instead of globally enabling Busy status for all commands here, the host can assert Busy status for selected commands by asserting the Busy bit in descriptor table Control Words for the individual commands. When response to a command conveys Busy status, the device suppresses transmission of data words that would normally accompany status transmission. For any message transacted with Busy status, the WASBUSY flag is asserted in the stored Message Information Word.

Bit No.	Mnemonic	R/W	Reset	Function
2	SSYSF	R/W	0	Subsystem Flag. This register bit is logically ORed with the SSYSF input pin. If either SSYSF register bit or SSYSF pin is asserted, the SSYSF Subsystem Flag status bit is set. If the Configuration Register 2 MCOPT1 bit equals 0, reception of a “transmit vector word” mode command (MC16) causes automatic reset of the SSYSF status bit in this register; when this occurs, the register bit is reset before status word transmission begins.
1	-----	R	0	Not used, this bit cannot be set.
0	TF	R/W	0	Terminal Flag. When this bit is asserted, the Terminal Flag status bit is set.

5.9. Time-Tag Register (0x0008)

This register is Read Only and is cleared after $\overline{\text{MR}}$ pin Master Reset or SRST software reset. Reads to this register address return the current value of the free running 16-bit Time Tag counter. Counter resolution is programmed by TTCK2:0 bits in Configuration Register 1. Options are: 2, 4, 8, 16, 32 and 64us, or externally provided clock.



The device automatically resets the Time-Tag count when a “synchronize” mode command without data (MC1) is received. In addition, the host can reset the Time-Tag count at any time by asserting the RTTAG bit in Configuration Register 2.

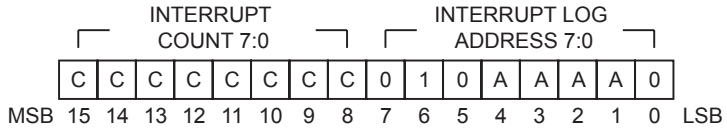
The MCOPT2 and MCOPT3 bits in Configuration Register 2 allow automatic loading of Time-Tag count using the data word received with a “synchronize with data” mode command, MC17. If both of these bits equal one, the data word received with a valid “synchronize” mode command (MC17) is unconditionally loaded into the Time-Tag counter. For non-broadcast MC17 commands, the counter load occurs before status word transmission. If both MCOPT2 and MCOPT3 bits equal 0, the external host assumes responsibility for actions needed to perform “synchronize” duties upon reception of the valid MC17 “synchronize” command, but status transmission automatically occurs.

The binary 01 and 10 combinations of the MCOPT2 and MCOPT3 bits support certain extended subaddressing schemes. If the MCOPT3-MCOPT2 bits equal 01, the received data word is automatically loaded into the Time-Tag counter if the low order bit of the received data word (bit 0) equals 0. If the MCOPT3-MCOPT2 bits equal 10, the received data word is automatically loaded into the Time-Tag counter if the low order bit of the received data word (bit 0) equals 1. For non-broadcast MC17 commands, the counter load occurs before status word transmission.

5.10. Interrupt Log Address Register (0x0009)

This 16-bit register is Read-Only and is fully maintained by HI-6120/21 logic. **The register contains 0x0040 after $\overline{\text{MR}}$ pin master reset but is not affected by SRST software reset.** Bits 7:0 contain an address pointer for the 32-word Interrupt Log Buffer located in shared RAM. The value in Interrupt Log Address register bits 7:0 indicates the storage address where interrupt information words will be stored for the next occurring interrupt, 0x40 - 0x5E. The value is always even since two words are stored for each interrupt.

Bits 15:8 contain a count value for the number of interrupts logged (0 - 255) since the Interrupt Log Address Register was last read. The count increment stops at 255. Bits 15:8 are reset automatically after this register is read by the host.

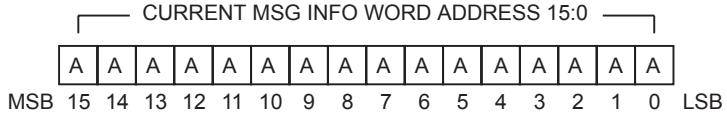


To help the host process interrupts, the device maintains information from the 16 most recent interrupts in a 32-word ring buffer in shared RAM, found at address range 0x0040 to 0x005F. Each interrupt stores two information words: the Interrupt Identification Word (IIW) identifies the interrupt type(s) that occurred; the Interrupt Address Word (IAW) identifies the interrupt source. For interrupts that result from message processing, the IAW contains the 16-bit address of the command's Control Word in the Descriptor Table. For hardware interrupts, the IAW value is 0x0000.

After $\overline{MR}$ master reset, the device automatically resets this register to 0x0040, an interrupt count of zero and log address of 0x40. During terminal operation, the host can read bits 15:8 to see the number of interrupts logged in the buffer since the last read operation upon the register. Information words for the sixteenth interrupt are stored in buffer addresses 0x005E and 0x005F, and the Interrupt Log Address "rolls over" to read 0x40, where interrupt information for the seventeenth interrupt will be stored. For further information on interrupts, see descriptions for the Interrupt Enable register, the Pending Interrupt register, and see the later section entitled "Interrupt Management".

5.11. Current Message Information Word Address Register (0x000A)

This 16-bit register is Read-Only and is fully maintained by the device. This register is cleared after $\overline{MR}$ pin master reset, but is not affected by SRST software reset. Also see "Current Control Word Address" register, 0x0004.

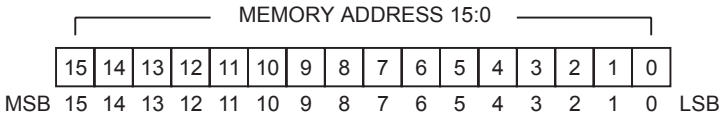


NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). This register is unaffected by software reset.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15-0	MIWA15:0	R/W	0	Current Message Information Word Address Register This register contains the data buffer address for the last command's Message Information Word, or MIW, corresponding to the current command stored in the Current Command Register (0x0003). This register is updated 5us after the ACTIVE output is asserted. Bit 15 is MSB.

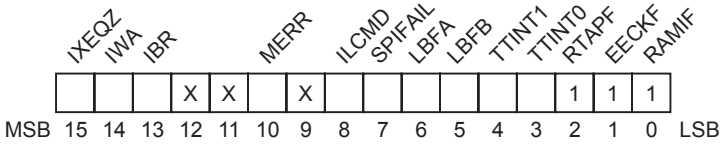
5.12. Memory Address Pointer Register (HI-6121 only) (0x000F)

This register is Read-Write and is cleared after $\overline{MR}$ pin master reset, but is not affected by SRST software reset. This register is maintained by the host. The contained value is a memory address used when fulfilling RAM or register read or write operations via the HI-6121 Serial Peripheral Interface (SPI). See data sheet section, "Host Serial Peripheral Interface (SPI)" for further details. For HI-6120 devices, writes to this address have no effect; the address reads back 0x0000 if a host read cycle occurs.



5.13. Interrupt Enable Register (0x0010)

This 16-bit register is Read-Write (except bits 2-0 are read only) and is fully maintained by the host. All bits are active high. For further information on interrupts, see descriptions for the Pending Interrupt and Interrupt Log Address registers, and refer to the later section entitled “Interrupt Management”.



An interrupt type is globally disabled when the corresponding bit in this register is reset. This allows the external host or subsystem to temporarily disable interrupt servicing for some or all interrupts. While an interrupt enable bit is negated, the terminal does not generate an interrupt output signal for the corresponding interrupt event. Note: Asserting an interrupt bit in this register after an event occurs does not generate an interrupt for that event. For some interrupts that result from message processing, interrupt enable bits in a each command’s descriptor Control Word act in combination with settings in this register to respond appropriately to interrupt-causing events.

NOTE: ‘*Reset*’ refers to bit value following Master Reset ($\overline{MR}$). This register is unaffected by software reset.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	IXEQZ	R/W	0	Index Equal Zero Interrupt. When this bit is asserted, interrupts are globally enabled for (a) subaddresses using indexed buffer mode when the index decrements from 1 to 0, and (b) subaddresses using a circular buffer mode when the pre-determined number of messages has been transacted. When this bit is asserted, occurrence of an IXEQZ event (a) or (b) causes $\overline{INTMES}$ output assertion (if the IXEQZ bit is set in the command’s descriptor Control Word).
14	IWA	R/W	0	Interrupt When Accessed Interrupt. When this bit is asserted, interrupts are globally enabled for each message occurrence to subaddresses in which the Descriptor Control Word allows the IWA interrupt. When this bit is asserted, occurrence of an IWA event causes $\overline{INTMES}$ output assertion (if the IWA bit is set in the command’s descriptor Control Word).
13	IBR	R/W	0	Broadcast Command Received Interrupt. When this bit is asserted, interrupts are globally enabled for each broadcast message to subaddresses in which the Descriptor Control Word allows the IBR interrupt. When this bit is asserted, occurrence of an IBR event causes $\overline{INTMES}$ output assertion (if the IBR bit is set in the command’s descriptor Control Word).
12,11	-----	R/W	0	Not Used.

Bit No.	Mnemonic	R/W	Reset	Function
10	MERR	R/W	0	Message Error Interrupt. When this bit is high, the $\overline{\text{INTMES}}$ interrupt output is asserted when a message error is detected. Errors are caused by Manchester encoding problems or protocol errors. Interrupt assertion occurs whenever the terminal sets the ME “message error” bit in the terminal’s status word. The detected error type can be found in Message Information Word stored as a result of message processing.
9	-----	R/W	0	Not Used.
8	ILCMD	R.W	0	Illegal Command Interrupt. Illegal commands are defined in the Illegalization Table. When enabled, the ILCMD interrupt is asserted when the Illegalization Table bit corresponding to the received command is logic 1. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. When illegal commands are received, the terminal responds by transmitting status word with ME “message error” flag set; no data words are transmitted. If this ILCMD bit is high, all illegal commands cause $\overline{\text{INTMES}}$ interrupt output assertion. See next section entitled “Pending Interrupt Register” (below) and the section entitled “Illegalization Table” for further information.
7	SPIFAIL	R.W	0	SPI Fail Interrupt (HI-6121 only). The HI-6121 uses a SPI interface for host access. The device operates in SPI Slave mode. When this bit is high, the $\overline{\text{INTHW}}$ output is asserted and the Interrupt Log is updated each time an incorrect number of SCK clocks occurs during SPI chip select assertion.
6,5	LBFA, LBFB	R/W	0	Loopback Fail Bus A and Loopback Fail Bus B Interrupts. During all transmitted command responses, the device compares words transmitted to the received and decoded words detected on the bus. When this bit is high, the $\overline{\text{INTMES}}$ output is asserted and the Interrupt Log is updated each time loopback detects word mismatch.
4	TTINT1	R/W	0	Time-Tag Interrupt 1. If this bit is logic 1, the $\overline{\text{INTHW}}$ interrupt output is asserted and the TTINT1 bit is set in the Pending Interrupt register each time the free-running Time-Tag counter value matches the value stored in the Time-Tag Utility Register.
3	TTINT0	R/W	0	Time-Tag Interrupt 0. If this bit is logic 1, the $\overline{\text{INTHW}}$ interrupt output is asserted and the TTINT0 bit is set in the Pending Interrupt register each time the free-running Time-Tag counter value rolls over from 0xFFFF full count to 0x0000.
2	RTAPF	R	1	RT Address Parity Fail Interrupt. When this bit is high, the $\overline{\text{INTHW}}$ interrupt is asserted when RT address parity error is detected. This bit is 1 after $\overline{\text{MR}}$ master reset and cannot be reset by host register write.

Bit No.	Mnemonic	R/W	Reset	Function
1	EECKF	R	1	Initialization EEPROM Checksum Fail Interrupt. When this bit is high, the $\overline{\text{INTHW}}$ interrupt is asserted if serial EEPROM checksum failure occurs during auto-initialization. This bit is 1 after $\overline{\text{MR}}$ master reset and cannot be reset by host register write.
0	RAMIF	R	1	RAM Initialization Fail Interrupt. When this bit is high, the $\overline{\text{INTHW}}$ interrupt is asserted after auto-initialization if an initialized RAM location does not match its 2 corresponding serial EEPROM locations. This bit is 1 after $\overline{\text{MR}}$ master reset and cannot be reset by host register write.

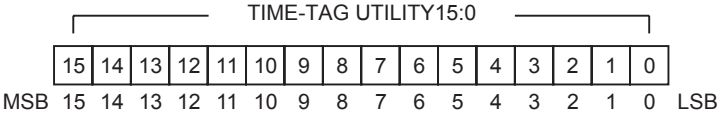
The Interrupt Enable Register lets the host temporarily or permanently disable interrupt servicing for some or all interrupt types. When bits are reset in this register, interrupt output signals are globally disabled for the corresponding interrupt types. Asserting a bit in the Interrupt Enable register after an event occurs does not generate an interrupt for that event. The IXEQZ, IWA and IBR interrupts result from message processing. The host can enable or disable these three interrupt types for individual subaddresses and mode code commands by setting or resetting the IXEQZ, IWA and IBR bits in descriptor table Control Words corresponding to each subaddress or mode command. While the ILCMD and MERR interrupts also result from message processing, these interrupts (along with all hardware interrupts) are globally enabled or disabled, and are unaffected by descriptor table settings. Table gives a summary of settings and responses to interrupt-causing messages.

Table 6. Settings and Responses to Interrupt-Causing Messages

SETTING		RESPONSE	
Descriptor Control Word IXEQZ, IWA & IBR Bits	**Interrupt Enable Register Bit for Interrupt Type**	**Effect on Corresponding Bit in Pending Interrupt Register**	**Is Interrupt Output Signal Generated**
Reset Set Set	Don't Care Reset Set	No Change No Change Pending Int. Register bit is set	No No Yes
All Interrupts Except IXEQZ, IWA & IBR (no Control Word bits)	Reset Set	No Change Pending Int. Register bit is set	No Yes

5.14. Time-Tag Utility Register (0x0011)

This 16-bit register is Read-Write and is fully maintained by the host. **This register is cleared after $\overline{\text{MR}}$ pin master reset, but is not affected by SRST software reset.** This register has two functions associated with the free-running Time-Tag counter:



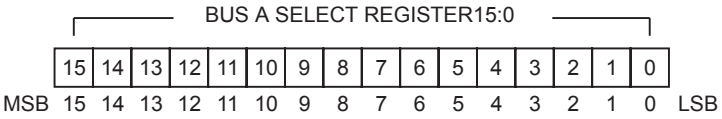
Function 1: When Configuration Register 2 is written causing a 0 to 1 transition of the TTLOAD bit, the value contained in the Time-Tag Utility register is loaded into the Time-Tag counter.

Function 2: If the TTINT1 bit in the Interrupt Enable register is set, the Interrupt Pending register TTINT1 bit is set and

the $\overline{\text{INTHW}}$ interrupt output is asserted each time the free-running Time-Tag counter value matches the value stored in the Time-Tag Utility register.

5.15. Bus A Select Register (0x0012)

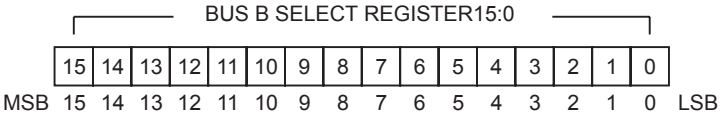
This 16-bit register is Read-Write and is fully maintained by the host. **This register is cleared after $\overline{\text{MR}}$ pin master reset, but is not affected by SRST software reset.** The Bus A Select register is only used when the MCOPT4 bit in Configuration Register 2 equals 0. This MCOPT4 setting means the device automatically fulfills mode commands MC20 (decimal) “selected transmitter shutdown” or MC21 “override selected transmitter shutdown”.



“Transmitter shutdown” or “shutdown override” can only occur for the inactive bus. If either mode command is received on Bus B, the inactive bus is Bus A. The device compares the received mode data word to the contents of the Bus A Select register to determine whether inactive Bus A is selected for “transmitter shutdown” or “transmitter shutdown override”. (Bus shutdown or shutdown override can only occur for the inactive bus.) If the data word matches the value stored in the Bus A Select register and MCOPT4 equals 0, the device automatically fulfills MC20 “transmitter shutdown” or MC21 “shutdown override” without host assistance: If the mode command received was MC20, the Transmit Shutdown A bit in the built-in test (BIT) word is asserted. If mode command MC21 was received, the Transmit Shutdown A bit in the BIT Word is negated. Refer to Configuration Register 2 description of MCOPT4 bit for additional details.

5.16. Bus B Select Register (0x0013)

This 16-bit register is Read-Write and is fully maintained by the host. **This register is cleared after $\overline{\text{MR}}$ pin master reset, but is not affected by SRST software reset.** The Bus B Select register is only used when the MCOPT4 bit in Configuration Register 2 equals 0. This MCOPT4 setting means the device automatically fulfills mode commands MC20 (decimal) “selected transmitter shutdown” or MC21 “override selected transmitter shutdown”.

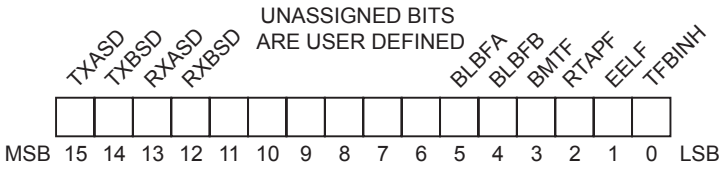


“Transmit shutdown” or “shutdown override” can only occur for the inactive bus. If either mode command is received on Bus A, the inactive bus is Bus B. The device compares the received mode data word to the contents of the Bus B Select register to determine whether inactive Bus B is selected for “transmitter shutdown” or “transmitter shutdown override”. If the data word matches the value stored in the Bus B Select register and MCOPT4 equals 0, the device automatically fulfills MC20 “transmit shutdown” or MC21 “shutdown override” without host assistance: If the mode command received was MC20, the Transmit Shutdown B bit in the built-in test (BIT) word is asserted. If mode command MC21 was received, the Transmit Shutdown B bit in the BIT Word is negated. Refer to Configuration Register 2 description of MCOPT4 bit for additional details.

5.17. Built-in Test Word Register (0x0014)

Bits 4-11 in this 16-bit register are read-write, the remaining bits are read-only. The ten assigned bits are written by

the device when predetermined events occur. The host may overwrite the device-written bits 5 and 4. After $\overline{MR}$ pin master reset, bits 13-12, 5-4 and 0 are reset. Bits 15-14 will be set if the corresponding TXINHA or TXINHB input pins are high. Bits 3-1 will be set if RT address parity error, or post-$\overline{MR}$ memory test or auto-initialization failure occurred.



If the ALTBITW option bit in Configuration Register 2 is zero when a valid "transmit BIT word" mode command (MC19) is received, the current value in this register is transmitted as the mode data word in the terminal response. The value is also copied to the assigned data buffer for MC19, after mode command fulfillment.

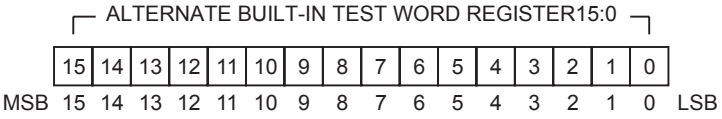
NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The value "PIN" denotes the bit is set to the value of the corresponding pin following Master Reset. The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15 14	TXASD TXBSD	R	PIN SR = PIN	Transmitter A Shutdown. Transmitter B Shutdown. These read-only bits are set when the corresponding bus transmitter was disabled by assertion of the bus TXINHA or TXINHB input pin, or by fulfillment of a "transmitter shutdown" mode command MC4 or MC20. Refer to the description for the SDSEL bit in Configuration Register 1 and the description for the MCOPT4 bit in Configuration Register 2 for further information.
13 12	RXASD RXBSD	R	0 SR = 0	Receiver A Shutdown. Receiver B Shutdown. These read-only bits are set when the corresponding bus receiver was disabled concurrently with the bus transmitter by a "transmitter shutdown" mode command MC4 or MC20. Refer to the description for the SDSEL bit in Configuration Register 1 and the description for the MCOPT4 bit in Configuration Register 2 for further information.
11-6	-----	R/W	0	User defined. Host can write any value.
5	BLBFA	R	0 SR = 0	Built-In-Self-Test (BIST) Loopback Fail Bus A (see Section 5.20). This bit is set if Bus A loopback failure error occurs during built-in self-test.
4	BLBFB	R	0 SR = 0	BIST Loopback Fail Bus B (see Section 5.20). This bit is set if Bus B loopback failure error occurs during built-in self-test
3	BMTF	R	Test Result	BIST Memory Test Fail (see Section 5.20). This bit is set if error occurs during built-in self-test for device RAM memory.
2	RTAPF	R	Test Result	RT Address Parity Failure. This bit is asserted when Operational Status Register bits 15:10 reflect parity error. After $\overline{MR}$ master reset, bits 15:10 in the Operational Status Register reflect input pin states, but will be overwritten if subsequent auto-initialization is performed (if AUTOEN pin is high) and the initialization EEPROM contains different data for Operational Status Register bits 15:10.

Bit No.	Mnemonic	R/W	Reset	Function
1	EELF	R	Test Result	Auto-Initialization EEPROM Load Fail. This bit only applies when auto-initialization is enabled (AUTOEN input pin state equals 1). This bit is set if, after $\overline{MR}$ master reset, failure occurs when copying serial EEPROM to registers and RAM. When this occurs, bit 0 or bit 1 will be set in the Operational Status Register (0x0002) to indicate type of failure.
0	TFBINH	R	0 SR = 0	Terminal Flag Bit Inhibited. This bit is set when the Terminal Flag status bit is disabled while fulfilling an “inhibit terminal flag bit” mode code command (MC6). This bit is reset if terminal flag status bit disablement is later cancelled by an “override inhibit terminal flag bit” mode code command (MC7).

5.18. Alternate Built-in Test Word Register (0x0015)

This 16-bit register is Read-Write and is fully maintained by the external host. **This register is cleared after $\overline{MR}$ pin master reset but is unaffected by SRST software reset.**



If the ALTBITW option bit in Configuration Register 2 equals one when a valid “transmit BIT word” mode command (MC19) is received, the current value in this register is transmitted as the mode data word in the terminal response. The value is also copied to the assigned data buffer for MC19, after mode command fulfillment.

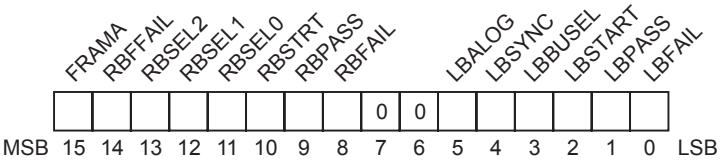
5.19. Reserved Register (0x0016)

Register 0x0016 is used for factory testing. **It is cleared after $\overline{MR}$ pin master reset and cannot be written by the host while the TEST input pin is low.**

5.20. Test Control Register (0x0017)

This register controls RAM built-in self-test, and transceiver loopback testing. Bits 0, 1, 8, 9 are Read Only. The remaining bits in this register are Read-Write but can be written only when the TEST input pin is high. If TEST = 0, these bits will read back 0x0000.

This register supports two types of test: Register bits 15 - 8 are used for RAM built-in self test (RAM BIST). Register bits 7 - 2 are used for transceiver loopback testing (either digital loopback or analog loopback).



Under internal logic control, this device uses one RAM self test (Inc / Dec Test described below) to check internal RAM memory after $\overline{MR}$ pin master reset. Test Control Register bits 15 - 8 provide a means for the host to perform RAM self-test at other times. Register bits 13:11 select RAM test type. Then bit 10 starts the selected RAM test, and bits 9-8 report a pass/fail result after test completion. All tests are destructive, overwriting data present before test commencement.

NOTE: '*Reset*' refers to bit value following either Master Reset ($\overline{MR}$) or software reset.

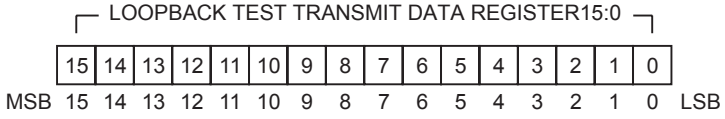
<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>15</td><td>FRAMA</td><td>R/W</td><td>0</td><td>Full RAM Access Enable.
During normal operation, some bits in certain RAM locations (e.g., Descriptor Table Control Words) cannot be written by the host. When the FRAMA bit is asserted, host writes to RAM are unrestricted to permit full testing. During normal completion, this bit must be reset to logic 0.</td></tr>
<tr><td>14</td><td>RBFFAIL</td><td>R/W</td><td>0</td><td>RAM BIST Force Failure.
When this bit is asserted, RAM test failure is forced to verify that RAM BIST logic is functional.</td></tr>
<tr><td>13,12,11</td><td>RBSEL2:0</td><td>R/W</td><td>0</td><td>RAM BIST Select Bits 2-0.
This 3-bit field selects the RAM BIST test mode applied when the RBSTART bit is set:
<table>
<tr><th>RBSEL2:0</th><th>Selected RAM Test</th><th>Test Time</th></tr>
<tr><td>000</td><td>Idle</td><td>-</td></tr>
<tr><td>001</td><td>Pattern Test, described below</td><td>14.42ms</td></tr>
<tr><td>010</td><td>Write 0x0000 to RAM address range 0x0000 - 0x7FFF</td><td>170µs</td></tr>
<tr><td>011</td><td>Read and verify 0x0000 over RAM address range 0x0000 - 0x7FFF</td><td>500µs</td></tr>
<tr><td>100</td><td>Write 0xFFFF to RAM address range 0x0000 - 0x7FFF</td><td>170µs</td></tr>
<tr><td>101</td><td>Read and verify 0xFFFF over RAM address range 0x0000 - 0x7FFF</td><td>500µs</td></tr>
<tr><td>110</td><td>Inc / Dec Test performs only steps 5 - 8 of the Pattern Test below</td><td>1.32ms</td></tr>
<tr><td>111</td><td>Idle</td><td>-</td></tr>
</table></td></tr>
</table>

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
13,12,11	RBSEL2:0 (continued)	R/W	0	**Description of the RAM BIST "PATTERN" test selected when register bits RBSEL2:0 = 001:** *Note: Test read /write accesses to addresses 0x0000 - 0x001F involve 32 RAM locations not accessible to the host. These accesses do not affect the host-accessible registers, overlaying the same address range.* 1. Write 0x0000 to all RAM locations, 0x0000 through 0x7FFF. 2. Repeat the following sequence for each RAM location from 0x00000 through 0x7FFF: a. Read and verify 0x0000 b. Write then read and verify 0x5555 c. Write then read and verify 0xAAAA d. Write then read and verify 0x3333 e. Write then read and verify 0xCCCC f. Write then read and verify 0x0F0F g. Write then read and verify 0xF0F0 h. Write then read and verify 0x00FF i. Write then read and verify 0xFF00 j. Write 0x0000 then increment RAM address and go to step (a) 3. Write 0xFFFF to all RAM locations, 0x0000 through 0x7FFF 4. Repeat the following sequence for each RAM location from 0x00000 through 0x7FFF: a. Read and verify 0xFFFF b. Write then read and verify 0x5555 c. Write then read and verify 0xAAAA d. Write then read and verify 0x3333 e. Write then read and verify 0xCCCC f. Write then read and verify 0x0F0F g. Write then read and verify 0xF0F0 h. Write then read and verify 0x00FF i. Write then read and verify 0xFF00 j. Write 0xFFFFthen increment RAM address and go to step (a) 5. Write each cell's memory address into each RAM location from 0x00020 to 0x7FFF. 6. Read each memory location from 0x00000 to 0x7FFF and verify it contains its address. 7. Write 1s complement of each cell's memory address, into each RAM location (same addr range). 8. Read each memory location and verify it contains the 1s complement of its address.
10	RBSTRT	R/W	0	RAM BIST Start. Writing logic 1 to this bit initiates the RAM BIST test selected by register bits RBSEL2:0. The RBSTRT bit can only be set if the TEST input pin is high and if register bit 15 is already asserted. This bit is automatically cleared upon test completion. Register bits 9-8 indicate pass / fail test result.

Bit No.	Mnemonic	R/W	Reset	Function
9	RBPASS	R	0	RAM BIST Pass. Device logic asserts this bit when the selected RAM test completes without error. This bit is automatically cleared when RBSTRT bit 10 is set.
8	RBFAIL	R	0	RAM BIST Fail. Device logic asserts this bit when failure occurs while performing the selected RAM test. This bit is automatically cleared when RBSTRT bit 10 is set. When BIST failure occurs, a clue to the failing RAM address can be read at register address 0x001E. For speed, the RAM BIST concurrently tests 4 quadrants of the RAM address range, in parallel. If test failure occurs, register address 0x001E contains the RAM address being tested in the lowest RAM quadrant. Actual failure will occur in any of these four locations: at RAM address “ADDR” stored in register 0x001E, or ADDR+0x2000, or ADDR+0x4000 or ADDR+0x6000.
7,6	-----	R	0	Not Used. These bits cannot be set. A READ will return 0x0000.
5	LBALOG	R/W	0	Loopback Test Analog. The device supports either digital or analog loopback testing for either bus transceiver. When the LBALOG bit is low, digital loopback is selected and no data is transmitted onto the selected external MIL-STD-1553 bus. When the LBALOG bit is high, analog loopback is selected and a test word is transmitted onto and received from the selected external MIL-STD-1553 bus.
4	LBSYNC	R/W	0	Loopback Test Word Sync Select. When the LBSYNC bit is high, the loopback test word is transmitted with command sync. When the LBSYNC bit is low, the loopback test word is transmitted with data sync.
3	LBBUSEL	R/W	0	Loopback Test Bus Select. When this bit is low, loopback testing occurs on Bus A. When this bit is high, loopback testing occurs on Bus B.
2	LBSTART	R/W	0	Loopback Test Start. Writing logic 1 to this bit initiates the loopback test selected by register bits 3, 4 and 5. The LBSTRT bit can only be set if the external TEST pin is already asserted, and is automatically cleared upon test completion. Register bits 1,0 indicate pass / fail test result.
1	LBPASS	R	0	Loopback Test Pass. Device logic asserts this bit when the selected Loopback test completes without error. This bit is automatically cleared when LBSTART bit 2 is set.
0	LBFAIL	R	0	Loopback Test Fail. Device logic asserts this bit when failure occurs while performing the selected loopback test. Failure is comprised of Manchester encoding error, parity error, wrong sync type or data mismatch. This bit is automatically cleared when LBSTART bit 2 is set.

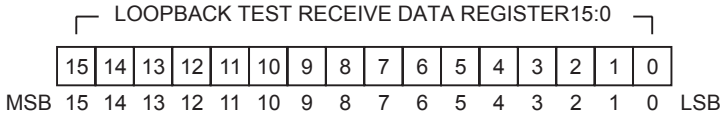
5.21. Loopback Test Transmit Data Register (0x0018)

This 16-bit register is Read-Write and is fully maintained by the host. **This register is cleared after $\overline{\text{MR}}$ pin master reset, but is not affected by SRST software reset.** The value contained in this register is used when performing digital loopback testing. See “Test Control Register (0x0017)”, for additional information.



5.22. Loopback Test Receive Data Register (0x0019)

This 16-bit register is Read-Only. **This register is cleared after $\overline{\text{MR}}$ pin master reset, but is not affected by SRST software reset.** Data is written to this register when performing digital loopback testing. See “Test Control Register (0x0017)”, for additional information.



6. COMMAND RESPONSES

A brief review of MIL-STD-1553 commands and responses is appropriate here to establish terminology used in the rest of this data sheet. Shown in Figure 3, each command word is comprised of a sync field, three 5-bit data fields, a single bit denoting Transmit / $\overline{\text{Receive}}$ direction and ends with a parity bit. The hardware decoder uses the sync field to determine word type (command vs. data). Word validity is based on proper sync encoding, Manchester II encoding, correct bit count and correct odd parity for the 16 data bits. Once a valid word with command sync is found, the sync and parity are stripped before the command's 16 data bits are stored for further processing.

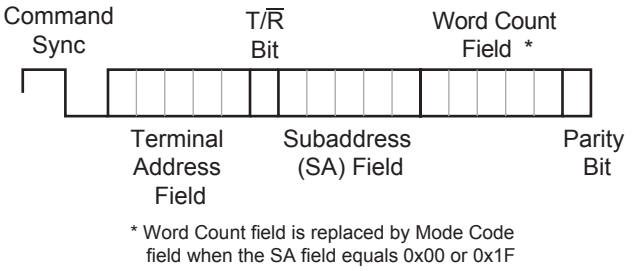


Figure 3. MIL-STD-1553 Command Word Structure

A "valid command" can be specifically addressed to the individual HI-6120 terminal (the command word's embedded Terminal Address field matches the terminal address latched in the Operational Status register) or can be a "broadcast command" addressed to all terminals. Broadcast commands are always addressed to RT address 31 (0x1F). In systems where broadcast commands are disallowed, RT31 is not used as a conventional terminal address. When set, the BCSTINV bit in Configuration Register 1 renders RT31 commands as "invalid": broadcast commands are indistinguishable from commands addressed to other terminals. Invalid commands are simply disregarded.

When the command word's 5-bit SA (subaddress) field is in the range of 1 to 30 (0x01 to 0x1E) the command is considered a "subaddress command". The terminal will either receive or transmit data words, and "direction" is specified by the command's T/$\overline{\text{R}}$ bit. The number of data words transacted is specified in the 5-bit word count field, ranging from 1 to 32 words. Thirty-two data words is represented when the word count field equals 0x00.

When the command's 5-bit subaddress field equals 0 or 31 (0x1F) a "mode code" command is indicated; the low order five bits no longer specify a word count, instead they convey a mode code value. This data sheet refers to mode code commands by the mode code number. For example, a mode command with 5-bit mode code field of 0x10 is called MC16, and the full range of mode code values is MC0 through MC31 (decimal).

Mode codes MC16 through MC31 (0x10 through 0x1F) have a single associated data word. When the command T/$\overline{\text{R}}$ bit equals 0, the data word is contiguous with the command word and received by the RT. When the command's T/$\overline{\text{R}}$ bit equals 1, the data word is transmitted by the RT, following the terminal's transmitted status word.

Mode codes MC0 through MC15 (0x0F) do not have associated data words. For these 16 commands, the command T/$\overline{\text{R}}$ bit does not specify "direction". These commands must be transmitted with T/$\overline{\text{R}}$ bit equal to 1. If the T/$\overline{\text{R}}$ bit is 0, the mode command is "undefined".

Twenty-two mode commands are "undefined mode commands " in MIL-STD-1553B:

Mode Codes 0 through 15 with T/R bit = 0
Mode Codes16, 18 and19 with T/R bit = 0
Mode Codes 17, 20 and 21 with T/R bit = 1

The UMCINV bit in Configuration Register 1 determines how these undefined mode commands are handled by the HI-6120/21. If the UMCINV configuration bit equals 1, the undefined mode commands are treated as invalid. They are not recognized by the device. There is no terminal response and status is not updated. If the UMCINV configuration bit equals 0, the 22 undefined mode commands are considered valid; this is the default condition following reset. For this case, terminal response depends on whether or not the application uses "illegal command detection."

If illegal command detection is not used, all Illegalization Table entries should be logic 0, including the 22 entries for these undefined commands. (The Illegalization Table is fully described in Section 7 on page 49. After $\overline{\text{MR}}$ reset, all entries equal logic 0.) The terminal responds "in form", transmitting clear status (and a single mode data word if the command is MC17, MC20 or MC21 with T/$\overline{\text{R}}$ bit = 1). Terminal status is updated.

If illegal command detection applies, the Illegalization Table entries for these 22 undefined commands should be initialized to logic 1. In this case, the terminal will respond with status word only, with Message Error bit set. No mode data word is transmitted. Terminal status is updated.

Twenty-seven mode codes are considered "reserved" in MIL-STD-1553B:

Mode Codes 9 through 15 with T/R bit = 1
Mode Codes 22 through 31 with T/R bit = 1
Mode Codes 22 through 31 with T/R bit = 0

Treatment of these reserved mode commands depends on their respective Illegalization Table entries. As described above for undefined mode commands, response depends on whether or not illegal command detection applies.

Any mode commands not implemented in the HI-6120/21 terminal should be treated the same as reserved mode commands. For example, command MC0 (with T/$\overline{R}$ = 1) is probably unimplemented because the HI-6120 does not have provisions for accepting “dynamic bus control”.

The important point is that “illegal command detection” should be universally applied (or not applied) when setting up a HI-6120/21 Remote Terminal application. Here are the two options:

Not using Illegal command detection. The HI-6120/21 Illegalization Table is left in its default state (all locations equal to $\overline{MR}$ post-reset 0x0000). The terminal responds “in form” to all valid commands, whether legal or illegal.

Using illegal command detection. The HI-6120/21 Illegalization Table is initialized by the host to implement “illegal command detection”. The host sets bits for all illegal commands. This generally includes the reserved and unimplemented mode commands, unimplemented subaddresses (or specific word counts, T/$\overline{R}$ bit states, and/or broadcast vs. non-broadcast status within subaddresses). Treatment for the undefined mode commands depends on UMCINV bit.

The host defines terminal response for all individual commands by initializing the Descriptor Table, fully described later. At this point, a few comments about the Descriptor Table are appropriate.

The command SA (subaddress) field has a range of 0 to 31 (0x1F). When SA is in the range 1 to 30 (0x1E), the command is a transmit or receive “subaddress command”. The number of data words transmitted or received is expressed in the low order 5 bits. When SA equals 0 or 31 (0x1F) the command is a mode command and the mode code value is expressed in the low order 5 bits.

For each subaddress, separate table “descriptor blocks” for transmit and receive commands permit different data buffering to be applied. The host initializes the table so each transmit-subaddress and each receive-subaddress uses one of four methods for storing message data. During table initialization, memory is allocated in shared RAM for storing message data according to the application requirements. Each transmit-subaddress and receive-subaddress has one or more data pointers (depending on buffer method) addressing its reserved data buffer(s).

Each mode command also has its own table “descriptor block”. Mode commands have either one data word or no associated data words. Descriptor words used as data pointers by “subaddress commands” are instead used for direct storage of transacted mode data words. Mode commands that transmit or receive mode data words have a dedicated storage address range in shared RAM, eliminating the need for descriptor table data pointers.

Each mode command with mode data word has its own fixed address for data storage. This includes reserved mode codes with data word. Thus the HI-6120/21 can respond consistently for all mode commands; transmitted data values for “in form” responses (when “illegal command detection” is not used) can be predetermined, even for the reserved mode commands.

6.1. RT to RT Commands.

The MIL-STD-1553 standard allows for data word transmission from a specified transmitting terminal to a different receiving terminal. When broadcast commands are allowed, data transmission can be addressed to the broadcast terminal address, RT31. If broadcast is allowed, the host should initialize the BCSTINV (broadcast invalid) bit in Configuration Register 1 to logic 0.

All RT to RT commands are characterized by a pair of contiguous command words: Command Word 1 is a receive command addressed to the intended receiving terminal, then Command Word 2 is a transmit command addressed to a single transmitting terminal. Command Word 2 cannot be broadcast address RT31. The HI-6120 automatically detects and handles RT to RT commands, except when either command word contains a subaddress field equal to 0x0 or 0x1F. Either subaddress value indicates a mode code command; the device treats RT to RT commands with mode code as invalid. If either RT-RT command word is addressed to the HI-6120/21 terminal but contains subaddress 0x0 or 0x1F, the command is not recognized; there is no RT command response, and no status updating for the benefit of following “transmit status” or “transmit last command” mode commands.

When either RT-RT command word (with subaddress field not equal to 0x0 or 0x1F) is addressed to the HI-6120/21 terminal, but the other command word contains subaddress 0x0 or 0x1F, the RT-RT command is not recognized as valid. There is no RT command response,

and no status updating for the benefit of following “transmit status” or “transmit last command” mode commands.

An RT-RT command pair where Command Word 1 is addressed to the HI-6120/21 terminal and Command Word 2 is addressed to a different terminal is considered an “RT-RT receive” command. When the message is transacted, the device sets the RTRT bit in the Receive Subaddress Message Information Word in the subaddress data buffer.

An RT-RT command pair where Command Word 2 is solely addressed to the HI-6120/21 terminal (not RT31) is considered an “RT-RT transmit” command. The Message Information Word does not distinguish the RT to RT transmit message from an ordinary RT to BC transmit command.

7. COMMAND ILLEGALIZATION TABLE

The following pages describe various structures residing in the RAM shared between the host and HI-6120 or HI-6121 command processing logic. The host initializes these structures to control the terminal’s response to received commands. The first structure described is the command Illegalization Table used for “illegal command detection”.

Illegal command detection is an optional process. When illegal command detection is not used, the terminal “responds in form” to all valid commands: it sends Clear Status and transacts the number of data words defined in the received command. When illegal command detection is not used, the bus controller cannot tell whether the command is legal or illegal, from the terminal’s transmitted response.

If illegal command detection is used, the terminal responds differently when an illegal command is detected. The terminal responds to illegal commands with “message error” status, transmitting only status word. Data word transmission is suppressed if the command type inherently includes transmitted data words. The terminal responds to each legal command with clear status and transacts the number of data words defined in the type of command received.

For consistency, apply illegal command detection to all illegal and unimplemented commands, and to all reserved or undefined mode code commands, or “respond in form” to all of these commands (illegal command detection disabled) by leaving the Illegalization Table in the all-cleared default state after $\overline{MR}$ master reset

The device uses a 256-word “Illegalization Table” in shared RAM to distinguish between legal and illegal commands. After the ($\overline{MR}$) master reset input is negated, HI-6120/21 performs internal self test including a shared RAM test which leaves all memory locations fully reset. Once self test is complete, the HI-6120/21 READY output goes high to indicate HI-6120/21 readiness for host initialization. At this point, all entries in the Illegalization Table read logic 0, so by default, illegal command detection is not applied.

To apply illegal command detection, the host (or auto-initialization) writes the Illegalization Table to set bits for all illegal command combinations. This typically includes any unimplemented subaddresses and/or word counts, undefined mode commands, reserved mode commands and any mode commands not implemented in the terminal design. Host initialization of the table can be replaced by auto-initialization.

Once STEX is set in Configuration Register 1, terminal execution begins. Each time a valid command is received, a 1-bit entry (indexed using command word data bits) is fetched from the Illegalization Table:

If fetched Illegalization Table bit equals logic 0, the command is “legal”; the terminal responds “in form”, transmitting clear status and transacting the number of data words defined for the message type. Terminal status is updated.

If fetched Illegalization Table bit equals logic 1, the command is “illegal”; the terminal responds with status word only, with Message Error bit set. No data words are transmitted. Terminal status is updated.

When illegal command detection is not applied, all table entries should read logic 0; the terminal responds “in form” to all valid commands.

The illegalization scheme allows any subset of command T/$\overline{R}$ bit, broadcast vs. non-broadcast status, subaddress and word count (or mode code number), for a total of 4,096 legal/illegal command combinations. Commands may be illegalized down to the word count level. For example, 10-word receive commands to a given subaddress may be legal, while 9-word receive commands to the same subaddress are illegal.

Broadcast receive commands are illegalized separately from non-broadcast receive commands. Transmit and receive commands for the same subaddress are illegalized separately. For mode commands, any combination of mode code number, T/$\overline{R}$ bit and broadcast/non-broadcast status can be legal or illegal.

The Illegalization Table is located in shared RAM within

the fixed address range of 0x0100 to 0x01FF. See Figure 4. The table is comprised of 256 16-bit words. To cover the full range of 1 to 32 data words, each subaddress uses a pair of illegalization registers. The lower register (even memory address) covers word counts 0 to 15, using one bit per word count. As in command encoding, “0” denotes 32 data words. Bit 0 corresponds to 32 data words, bit 1 corresponds to 1 data word and bit 15 corresponds to 15 data words. The upper register (odd memory address) similarly covers word counts 16 to 31, using one bit per word count. Bit 0 corresponds to 16 data words, while bit 15 corresponds to 31 data words.

When a command’s subaddress field equals 0 or 31 (0x1F), the command is a mode command. Table entries for mode commands use bits to represent mode code numbers, not word counts. The lower register (even memory address) covers mode codes 0 to 15, using one bit per mode code. Bit 0 corresponds to mode code 0, bit 15 corresponds to mode code 15. The upper register (odd memory address) similarly covers mode codes 16 to 31, using one bit per mode code. Bit 0 corresponds to mode code 16, bit 15 corresponds to mode code 31. There is no functional difference between SA0 mode commands and SA31 mode commands. Since either subaddress indicates a mode command, the subaddress 0 table words should match the subaddress 31 table words in each quadrant.

Table entries from 0x0142 to 0x017D do not have to be programmed. These correspond to broadcast transmit subaddress commands (undefined by MIL-STD-1553B) and are always invalid. There is no terminal response.

Addressing for the Illegalization Table is derived from the command word T/$\overline{R}$ bit, subaddress field, MSB of the Word Count (Mode Code) field and the command’s broadcast vs. non-broadcast status as shown below in Figure 4.

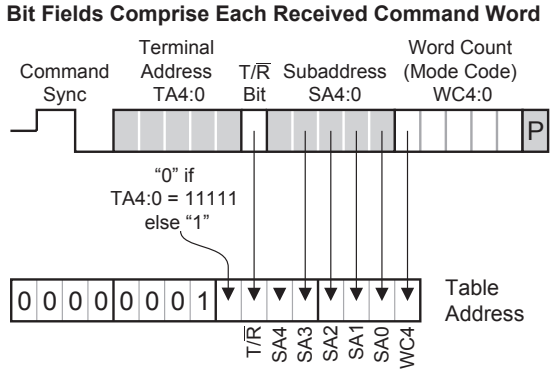


Figure 4. Deriving the Illegalization Table Address From the Received Command Word

Figure 6 shows individual bit locations in the Illegalization Table for broadcast and non-broadcast variants of all mode commands defined by MIL-STD-1553B. Locations are also identifed for reserved mode codes and undefined mode code commands.

The following examples illustrate how the Illegalization Table is initialized to distinguish between legal and illegal commands when “illegal command detection” is being used. Remember: If the terminal does not use illegal command detection, the table is left in its post-$\overline{MR}$ reset state, with all table locations reset to 0x0000. In this case, all command responses are “in form”.

For “subaddress commands” (ordinary receive commands or transmit commands) individual table bits correspond to word counts specified in the received command word. If a bit is 0, the corresponding word count is legal. If a bit is 1, the corresponding word count is illegal.

For example, transmit commands to subaddress 1 are controlled by the words at 0x01C2 and 0x01C3. In Figure 5, these words are located in the “RT Address Transmit” block. The word stored at 0x01C3 controls subaddress 1 transmit commands having word counts 16 to 31. The word stored at 0x01C2 controls subaddress 1 transmit commands having word counts 1 to 15 or 32. (Reminder: In MIL-STD-1553B, zero corresponds to 32 words.)

```
Word at 0x01C3 (Tx Subaddr 1) 31 to 16 words
Bit      15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
Words    31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

Word at 0x01C2 (Tx Subaddr 1) 15 to 1 & 32 words
Bit      15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
Words    15 14 13 12 11 10  9  8  7  6  5  4  3  2  1 32
```

If the word stored at 0x01C3 = 0xFFFF and the word stored at 0x01C2 = 0xFF0F, then commands with 4, 5, 6, or 7 data words are the only legal transmit commands for subaddress 1 and all other word counts are illegal. Receive commands and broadcast receive commands for Subaddresses1 through 30 are encoded similarly.

For “mode code commands” (characterized by command word subaddress field equal to 00000 or 11111 binary) individual table bits correspond to individual mode code values. Here “transmit” and “receive” simply indicate the state of the command word T/$\overline{R}$ bit. (For mode codes 0-15, the T/$\overline{R}$ bit does not indicate data direction since data is not transacted when fulfilling these commands).

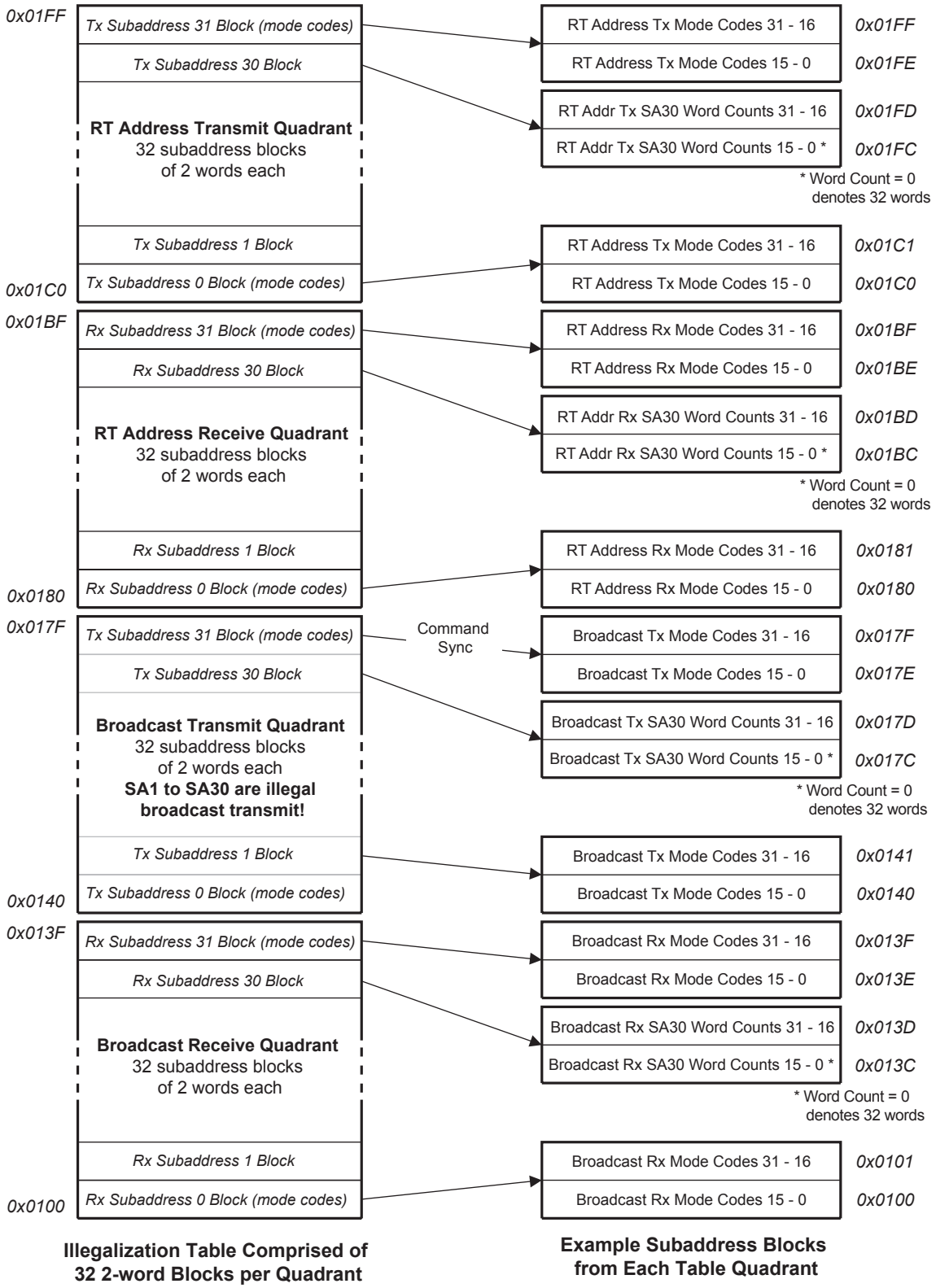


Figure 5. Fixed Address Mapping for Illegalization Table

Figure 6 summarizes the 16 Illegalization Table locations for mode commands. These locations are scattered through-

out the overall Illegalization Table shown in Figure 5. Remember: the host must initialize all table locations corresponding to both subaddress 0 and subaddress 31 (11111 binary).

Consider an example in which all reserved and all undefined mode commands are illegal. If all defined transmit mode commands are legal except MC0 (”dynamic bus control”) the eight table entries for transmit mode commands would be:

0x01FF and 0x01C1 = 1111 1111 1111 0010 = 0xFFF2
0x01FE and 0x01C0 = 1111 1110 0000 0001 = 0xFE01
0x017F and 0x0141 = 1111 1111 1111 1111 = 0xFFFF
0x017E and 0x0140 = 1111 1110 0000 0101 = 0xFE05

The receive mode command words are encoded similarly. Continuing the same example where all reserved and all undefined mode commands are illegal: If all defined receive mode commands are legal, the eight table entries for receive mode commands would be:

0x01BF and 0x0181 = 1111 1111 1100 1101 = 0xFFCD
0x01BE and 0x0180 = 1111 1111 1111 1111 = 0xFFFF
0x013F and 0x0101 = 1111 1111 1100 1101 = 0xFFCD
0x013E and 0x0100 = 1111 1111 1111 1111 = 0xFFFF

RAM Address		Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x01FF and 0x01C1	Tx MC31 - MC16	**MC #**	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Transmit Mode Commands With Data		**Status**	R	R	R	R	R	R	R	R	R	R	U	U	D	D	U	D
0x01FE and 0x01C0	Tx MC15 - MC0	**MC #**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transmit Mode Commands Without Data		**Status**	R	R	R	R	R	R	R	D	D	D	D	D	D	D	D	D
0x01BF and 0x0181	Rx MC31 - MC16	**MC #**	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Receive Mode Commands With Data		**Status**	R	R	R	R	R	R	R	R	R	R	D	D	U	U	D	U
0x01BE and 0x0180	Rx MC15 - MC0	**MC #**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Receive Mode Commands Without Data		**Status**	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
0x017F and 0x0141	Br.Tx MC31 - MC16	**MC #**	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Broadcast Transmit Mode Commands With Data		**Status**	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	U	U	NB	NB	U	NB
0x017E and 0x0140	Br.Tx MC15 - MC0	**MC #**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Broadcast Transmit Mode Commands Without Data		**Status**	R	R	R	R	R	R	R	D	D	D	D	D	D	NB	D	NB
0x013F and 0x0101	Br.Rx MC31 - MC16	**MC #**	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Broadcast Receive Mode Commands With Data		**Status**	R	R	R	R	R	R	R	R	R	R	D	D	U	U	D	U
0x013E and 0x0100	Br.Rx MC15 - MC0	**MC #**	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Broadcast Receive Mode Commands Without Data		**Status**	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

LEGEND
D = Defined Mode Command R = Reserved Mode Code
U = Undefined Mode Command NB = Broadcast Not Allowed

Figure 6. Summary of Illegalization Table Addresses for Mode Code Commands

8. TEMPORARY RECEIVE DATA BUFFER

The 32-word temporary receive data buffer resides in shared RAM in address space 0x0020 to 0x003F. The device optionally uses this buffer for temporary storage of receive data words until successful message completion. To enable the buffer, the host asserts the TRXDC bit in Configuration Register 2.

When enabled, the terminal stores received data words in the 32-word buffer during message processing. Upon error-free message completion, all buffered words are written in a burst to the data buffer memory assigned to the specific subaddress in the Descriptor Table.

When the TRXDB bit in Configuration Register 2 is negated, the temporary receive data buffer is disabled. At 20us intervals, the terminal writes received data words to assigned subaddress data buffer memory as each word is received. If message error occurs during data reception, data integrity is lost; valid data from the prior receive message may be partially overwritten by data from a message ending in error. MIL-STD-1553 states that all received data from messages ending in error **should be disregarded.**

In a typical application, the temporary buffer is not directly accessed by the host, although there is no restriction preventing host data access. The host should never write data into the temporary buffer space.

9. INTERRUPT LOG BUFFER

Two interrupt output pins notify the host upon occurrence of pre-determined interrupt-causing events. The interrupt types are listed below. Each interrupt type only occurs when the corresponding interrupt type bit is asserted in the Interrupt Enable Register. To manage host interrupts, the device architecture uses an Interrupt Log buffer, three control registers, two interrupt output pins and two interrupt acknowledge input pins. The data sheet section entitled “Interrupt Management” provides additional details.

Shown in Figure 7, the Interrupt Log Buffer is a 32-word ring buffer located in shared RAM, at address range 0x0040 to 0x005F. To help the host process interrupts, the device interrupt manager maintains information from the 16 most recent interrupts in this buffer. The buffer contains two information words for each occurring interrupt: the Interrupt Identification Word and Interrupt Address Word.

The Interrupt Identification Word (IIW) identifies the occurring interrupt type using a word format identical to the Pending Interrupt Register. Upon update, all bits except the occurring interrupt type bit(s) are reset.

Table 7. Interrupt Information Word Bits Summary

IIW - Interrupt Information Word			**IAW - Interrupt Address Word**
Bit	*Interrupt*	*Origin*	
15	IXEQZ	Message	IAW contains the Command Word Descriptor Table Address
14	IWA	Message	
13	IBR	Message	
12		-----	
11		-----	
10	MERR	Message	
9		-----	
8	ILCMD	Message	
7	SPIFAIL	Hardware	IAW contains 0x0000
6	LBFA	Hardware	
5	LBFB	Hardware	
4	TTINT1	Hardware	
3	TTINT0	Hardware	
2	RTAPF	Hardware	
1	EECKF	Hardware	
0	RAMIF	Hardware	

More than one bit may be asserted in an Interrupt Identification Word. For example, IBR (interrupt broadcast received) and MERR (interrupt message error) can occur for the same message. One assertion of the $\overline{\text{INTMES}}$ output pin alerts the host when concurrent message interrupts occur.

The Interrupt Address Word (IAW) identifies the originating command for message-based interrupts. When interrupts originate from message processing, the Interrupt Address Word (IAW) identifies the interrupt source using the 16-bit address of the command’s Control Word in the Descriptor Table. Hardware interrupts are not linked with command processing. These interrupts write an Interrupt Address Word value of 0x0000.

After $\overline{MR}$ reset or SRST software reset, the device automatically initializes bits 7:0 in the Interrupt Log Address register to the buffer's base address, 0x0040. The bit 7:0 value read will always be even, ranging from 0x0040 to 0x005E. Once terminal operation begins, the current value of the Interrupt Log Address indicates where the Interrupt Information Word (IIW) for the next occurring interrupt will be stored.

On the first interrupt occurring after reset, the device writes the IIW and IAW to offset locations 00000 and 00001 respectively. The device increments the ring buffer pointer after each word is stored, storing interrupt information sequentially in the ring buffer. Information words for the sixteenth interrupt are stored in offset locations 0x1E and 0x1F (buffer addresses 0x005E and 0x005F) and the Interrupt Log Address "rolls over" to again point to offset location 0 (buffer address 0x0040) where the Interrupt Information Word for the seventeenth interrupt will be stored.

Bits 15:8 in the Interrupt Log Address register maintain a count of interrupt events since the register was last read. The interrupt count stops at 255 decimal. Counts greater than 16 indicate buffer overrun, but the extended count capacity is provided as a diagnostic aid.

0x005F	INTERRUPT 16	Interrupt Address Word
0x005E	INTERRUPT 16	Interrupt Information Word
0x005D	INTERRUPT 15	Interrupt Address Word
0x005C	INTERRUPT 15	Interrupt Information Word
0x005B	INTERRUPT 14	Interrupt Address Word
0x005A	INTERRUPT 14	Interrupt Information Word
0x0059	INTERRUPT 13	Interrupt Address Word
0x0058	INTERRUPT 13	Interrupt Information Word
0x0057	INTERRUPT 12	Interrupt Address Word
0x0056	INTERRUPT 12	Interrupt Information Word
0x0055	INTERRUPT 11	Interrupt Address Word
0x0054	INTERRUPT 11	Interrupt Information Word
0x0053	INTERRUPT 10	Interrupt Address Word
0x0052	INTERRUPT 10	Interrupt Information Word
0x0051	INTERRUPT 9	Interrupt Address Word
0x0050	INTERRUPT 9	Interrupt Information Word
0x004F	INTERRUPT 8	Interrupt Address Word
0x004E	INTERRUPT 8	Interrupt Information Word
0x004D	INTERRUPT 7	Interrupt Address Word
0x004C	INTERRUPT 7	Interrupt Information Word
0x004B	INTERRUPT 6	Interrupt Address Word
0x004A	INTERRUPT 6	Interrupt Information Word
0x0049	INTERRUPT 5	Interrupt Address Word
0x0048	INTERRUPT 5	Interrupt Information Word
0x0047	INTERRUPT 4	Interrupt Address Word
0x0046	INTERRUPT 4	Interrupt Information Word
0x0045	INTERRUPT 3	Interrupt Address Word
0x0044	INTERRUPT 3	Interrupt Information Word
0x0043	INTERRUPT 2	Interrupt Address Word
0x0042	INTERRUPT 2	Interrupt Information Word
0x0041	INTERRUPT 1	Interrupt Address Word
0x0040	INTERRUPT 1	Interrupt Information Word

The Interrupt Log Address Register points to this address after Interrupt 15 event occurs. Upon Interrupt 16 completion, device logic reinitializes the log address pointer to 0x0040 before Interrupt 17 is processed.

EXAMPLE: 2-WORD LOG BUFFER ENTRIES FOR VARIOUS INTERRUPT TYPES...

Example 1: MERR bit is set in Interrupt Enable Register. An error occurs while transacting a receive command for subaddress 30:

Address Word = 0x0278 Descriptor Address for Rx Subaddress 30.*
Information Word = 0x0400 MERR (interrupt message error) bit = 1.

Example 2: IWA bit is set in Interrupt Enable Register. The IWA bit is set in Transmit Subaddress 30 Control Word to generate an interrupt upon each message occurrence. A transmit command is received for subaddress 30:

Address Word = 0x02F8 Descriptor Address for Tx Subaddress 30.*
Information Word = 0x4000 IWA (interrupt when accessed) bit = 1.

Example 3: ILCMD bit is set in Interrupt Enable Register. "Illegal Command Detection" is being applied and all Illegalization Table bits for undefined mode codes are set. An undefined Mode Code 0 with T/$\overline{R}$ bit = 0 is received:

Address Word = 0x0300 Descriptor Address for Rx Mode Code 0.*
Information Word = 0x0100 ILCMD (interrupt illegal command) bit = 1.

Example 4: TTINT0 bit is set in Interrupt Enable Register. The Time-Tag counter rolls over from full count 0xFFFF to 0x0000:

Address Word = 0x0000 (all hardware interrupts reset the IAW)
Information Word = 0x0010 TTINT0 (Time-Tag interrupt 0) bit = 1

* Figure 8 shows where these addresses occur in the Descriptor Table.

Interrupt Log Address Register is initialized by device logic to point to this address after hardware reset ($\overline{MR}$) or software reset

Figure 7. Fixed Address Mapping for Interrupt Log Buffer

10. DESCRIPTOR TABLE

The Descriptor Table, resides in shared RAM, in address range 0x0200 to 0x03FF. This table is initialized by the host (or auto-initialization) to define how the terminal processes valid commands. Descriptor Table settings for each command specify where message data is stored, how data is stored, whether host interrupts are generated, and other aspects essential to command processing. Shown in Figure 8, the table consists of 128 consecutive “descriptor blocks”, each comprised of four 16-bit words. The table is organized into four quadrants.

The Receive Subaddress and Transmit Subaddress quadrants define response for commands having a subaddress field ranging from 1 to 30 (0x1E). These are simple N-data word receive or transmit commands, where N can range from 1 to 32 words. When the command T/$\overline{R}$ bit equals 0, the receive command quadrant applies. When the T/$\overline{R}$ bit equals 1, the transmit command quadrant applies.

Both subaddress quadrants are padded at top and bottom with unused Descriptor Blocks for subaddresses 0 and 31 (0x1F). The word space reserved for SA0 and SA31 aligns the table addressing, but values stored in these eight locations is not used. Command subaddresses 0 and 31 indicate mode commands. The response for commands containing either SA value is defined in the two mode command table quadrants. The Receive Mode Command quadrant applies when the command word T/$\overline{R}$ bit equals 0, while the Transmit Mode Command quadrants applies when T/$\overline{R}$ equals 1.

The term “Transmit Mode Command” is a misnomer. All defined mode commands with mode code less than 0x0F haveT/$\overline{R}$ bit equal to 1, yet none of these mode commands transmits a data word. They transmit only the terminal status word, just like receive commands.

Within the Receive and Transmit Mode Command quadrants, block addressing is based on the low order 5 bits in the command word, containing the mode code value. This is fundamentally different from the Subaddress quadrants in which block addressing is based on the 5-bit subaddress field. Figure 9 shows how to derive Control Word address from the received Command Word. The Control Word address for the last valid command can also be found in the Current Control Word Address register.

All 128 4-word Descriptor Blocks start with a Control Word. There are four Control Word variants (described later), based on command type: receive vs. transmit and mode vs. non-mode commands. All descriptor Control Words are initialized by the host (or auto-initialization) to define basic command response. Each Control Word specifies the data buffer method and host interrupt for a specific subaddress or mode command.

Each subaddress has both a Receive Subaddress block and a Transmit Subaddress block. Receive and transmit commands to the same subaddress can be programmed to respond differently.

The function of the three remaining descriptor words (in each 4-word block) depends on the data buffer method specified in the Control Word. There are 4 data buffer options available:

Indexed (or Single Buffer) Method where a predetermined number of messages is transacted using a single data buffer in shared RAM. Several host interrupt options are offered, including an interrupt generated when all N messages are successfully completed.

Double (or Ping-Pong) Buffer Method where successive messages alternate between two data buffers in shared RAM. Several host interrupt options are offered.

Circular Buffer Mode 1 where buffer boundaries determine when the bulk transfer is complete and message information and time-tag words are stored with message data in a common buffer. Several host interrupt options are offered, including an interrupt generated when the allocated data buffer is full.

Circular Buffer Mode 2 where the number of messages transacted defines bulk transfer progress, and message data words are stored contiguously in one buffer while message information and time-tag words are stored in a separate buffer. Several host interrupt options are offered, including an interrupt generated when all N messages are successfully completed.

The 4-word Descriptor Table entry for each command (its descriptor block) begins with a Control Word. There are four types of descriptor Control Word:

- Receive Subaddress Control Word
- Transmit Subaddress Control Word
- Receive Mode Command Control Word
- Transmit Mode Command Control Word

The descriptor Control Word is initialized by the host to select data buffer method and interrupt options. After a command is processed by the HI-6120/21 terminal, the device updates the command’s descriptor Control Word. Update will differ based on the chosen data buffer method. Reading the descriptor table can differ from other RAM accesses. For HI-6120, see Section 15.1.1. For HI-6121, see Sections 15.2.5 and 15.2.7.

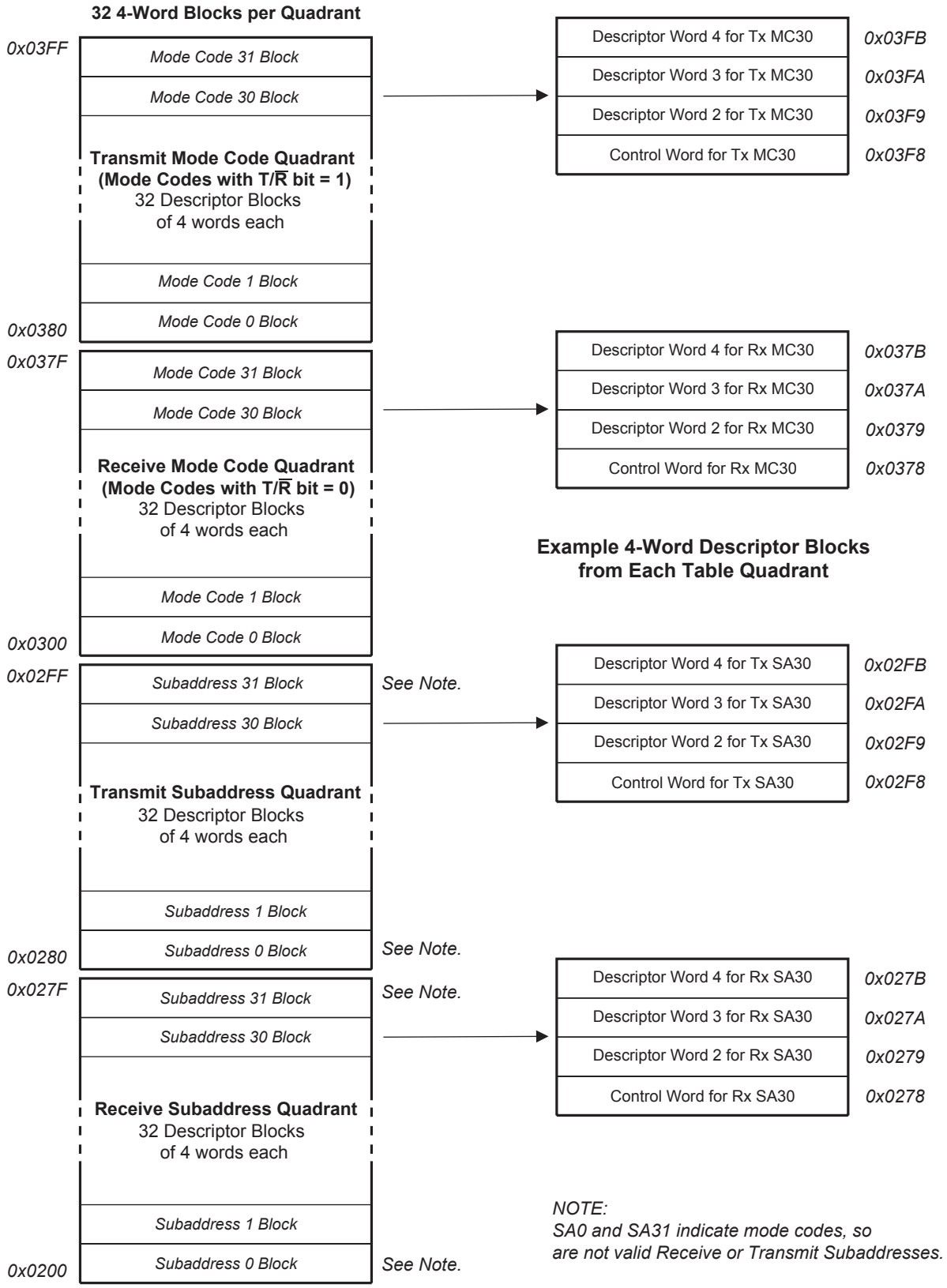


Figure 8. Address Mapping for Descriptor Table
(assumes table base address = 0x0200)

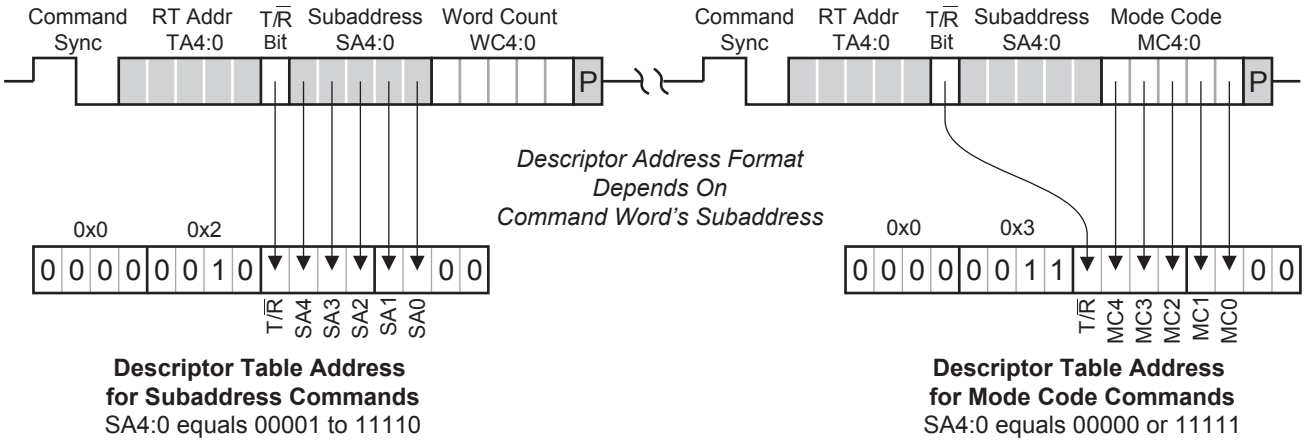
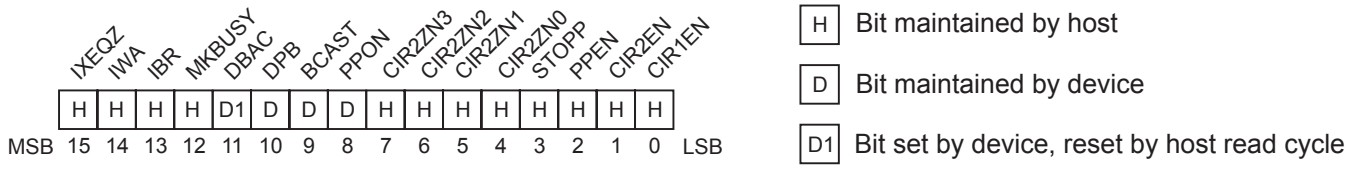


Figure 9. Deriving a Descriptor Table Control Word Address From Command Word
(assumes table base address = 0x0200)

10.1. Receive Subaddress Control Word

Receive Subaddress Control Words apply when a valid command word T/$\overline{R}$ bit equals zero (receive) and the subaddress field has a value in the range of 1 to 30 (0x1E). The descriptor Control Word defines terminal command response and interrupt behavior, and conveys activity status to the host. It is initialized by the host before terminal execution begins. Bits 8-11 cannot be written by the host; these bits are updated by the device during terminal execution, that is, when Configuration Register 1 STEX bit equals 1. The host can write bits 0-2 and 4-7 only when STEX equals zero; bits 3 and 12-15 can be written anytime. This register is cleared to 0x0000 by $\overline{MR}$ master reset. Software reset (SRST) clears just the DBAC, DPB and BCAST bits. **Following any read cycle to the Control Word address, the DBAC bit is reset.**



NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	IXEQZ		0	Interrupt When Index Equals Zero. If the Interrupt Enable Register IXEQZ bit is high, assertion of this bit enables generation of an interrupt for (a) subaddresses using indexed buffer mode when the INDX value decrements from 1 to 0, or (b) subaddresses using a circular buffer mode when the pre-determined number of messages has been transacted. If enabled, upon completion of command processing that results in index = 0, an IXEQZ interrupt is entered in the Pending Interrupt Register, output pin $\overline{INTMES}$ is asserted, and the interrupt is registered in the Interrupt Log.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
14	IWA		0	Interrupt When Accessed. If the Interrupt Enable Register IWA bit is high, assertion of this bit enables interrupt generation when the subaddress receives any valid receive command. If enabled, upon completion of command processing, an IWA interrupt is entered in the Pending Interrupt Register, output pin $\overline{\text{INTMES}}$ is asserted, and the interrupt is registered in the Interrupt Log.
13	IBR		0	Interrupt Broadcast Received. If the Interrupt Enable Register IBR bit is high, assertion of this bit enables interrupt generation when the subaddress receives a valid broadcast command. If enabled, upon completion of message processing an IBR interrupt is entered in the Pending Interrupt Register, output pin $\overline{\text{INTMES}}$ is asserted, and the interrupt is registered in the Interrupt Log. This bit has no function if the BCSTINV bit is high in Configuration Register 1. In this case, commands to RT address 31 are not recognized as valid by the device.
12	MKBUSY		0	Make Busy. The host asserts the MKBUSY bit to respond with Busy status for commands to this receive subaddress. This bit is an alternative to globally applying Busy status for all valid commands, enabled from the 1553 Status Bits Register. See that register description for additional information. When Busy is asserted, received data words are not stored and the DPB bit does not toggle after message completion.
11	DBAC		0 SR = 0	Descriptor Block Accessed. Internal device logic asserts the DBAC bit upon completion of message processing. The host may poll this bit to detect subaddress activity, instead of using host interrupts. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset, SRST software reset or a read cycle to this memory address.
10	DPB		0 SR = 0	Data Pointer B. This status bit is maintained by the device and only applies in ping-pong buffer mode. This bit indicates the buffer to be used for the next occurring receive command to this subaddress. When the DPB bit is logic 0, the next message will use Data Pointer A; when DPB is logic 1, the next message uses Data Pointer B. In ping-pong buffer mode, the bit is inverted after each **error-free** message completion. The DPB bit is not altered after messages ending in error, after illegal commands or after messages when the terminal responds with Busy status. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset or SRST software reset; therefore the first message received after either reset will use Buffer A. This bit is “don’t care” for indexed single-buffer mode or either circular buffer mode.
9	BCAST		0 SR = 0	Broadcast Command. Device logic sets this bit when a valid broadcast receive command is received at this subaddress. If IBR bit 13 and Interrupt Enable Register IBR bit are both set, the output pin $\overline{\text{INTMES}}$ is asserted. This bit has no function if the BCSTINV bit is asserted in the Configuration Register 1; in this case commands to RT address 31 are not recognized as valid by the device. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset or SRST software reset.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>8</td><td>PPON</td><td></td><td>0</td><td>Ping-Pong Enable Acknowledge.

This bit is controlled by the device and cannot be written by the host. It only applies if PPEN bit 2 was initialized to logic one by the host after reset, enabling ping-pong buffer mode for this subaddress. Device logic asserts this bit when it recognizes ping-pong is active for this subaddress. Before off-loading the receive data buffer for this subaddress, the host can ask the device to temporarily disable ping-pong by asserting STOPP bit 3. The device acknowledges ping-pong is disabled by negating PPON. The host can safely off-load the buffer without data collision while PPON is negated. After buffer servicing, the host asks the device to re-enable ping-pong by negating STOPP bit 3. The device acknowledges ping-pong is re-enabled by asserting PPON.

If PPEN bit 2 is high and PPON bit 8 is low when new commands arrive for this subaddress, ping-pong is disabled. Each new message overwrites existing data in the buffer specified by DPB bit 10, and the DPB bit does not toggle after command completion.</td></tr>
<tr><td>7-4</td><td>CIR2ZN</td><td></td><td>0</td><td>Circular Mode 2 Zero Number.

Used only in circular buffer mode 2, this 4-bit field is initialized with the number of trailing zeros in the initialized MIBA address. This is explained in Section 11.6, which fully describes circular buffer mode 2.</td></tr>
<tr><td>3</td><td>STOPP</td><td></td><td>0</td><td>Stop Ping-Pong Request.

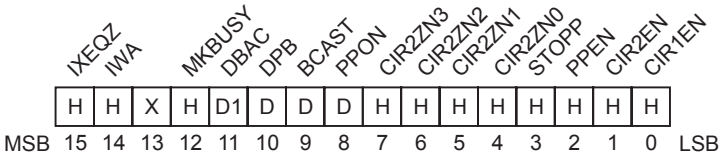
The host asserts this bit to suspend ping-pong buffering for this subaddress. The host resets this bit to ask the device to re-enable ping-pong. The device confirms recognition of ping-pong enable or disable status by writing PPON bit 8. Refer to later section fully describing ping-pong mode.</td></tr>
<tr><td>2
1
0</td><td>PPEN
CIR2EN
CIR1EN</td><td></td><td>0
0
0</td><td>Ping-Pong, Circular Buffer Mode 2 or Circular Buffer Mode 1 Enable.

The PPEN, CIR2EN and CIR1EN bits are initialized by the host to select buffer mode. The table below summarizes how buffer mode selection is encoded.

In the case of ping-pong, the host initializes the PPEN bit to logic one after reset to enable ping-pong buffering for this subaddress. The host asserts STOPP bit 3 to ask the device to temporarily disable ping-pong. Negating the STOPP bit asks the device to re-enable ping-pong. The device confirms ping-pong enable or disable state changes by writing the PPON bit.
<table>
<tr><th>PPEN</th><th>CIR2EN</th><th>CIR1EN</th><th>Buffer Mode</th></tr>
<tr><td>1</td><td>Don’t Care</td><td>Don’t Care</td><td>Ping-Pong</td></tr>
<tr><td>0</td><td>1</td><td>Don’t Care</td><td>Circular Mode 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Circular Mode 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Indexed Single Buffer</td></tr>
</table>
</td></tr>
</table>

10.2. Transmit Subaddress Control Word

Transmit Subaddress Control Words apply when a valid command word T/$\overline{R}$ bit equals one (transmit) and the subaddress field has a value in the range of 1 to 30 (0x1E). The descriptor Control Word defines terminal command response and interrupt behavior, and conveys activity status to the host. It is initialized by the host before terminal execution begins. Bits 8-11 cannot be written by the host; these bits are updated by the device during terminal execution, that is, when Configuration Register 1 STEX bit equals 1. The host can write bits 0-2 and 4-7 only when STEX equals zero; bits 3,12 and 14-15 can be written anytime. This register is cleared to 0x0000 by $\overline{MR}$ master reset. Software reset (SRST) clears just the DBAC, DPB and BCAST bits. **Following any host read cycle to the Control Word address, the DBAC bit is reset.**



H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	IXEQZ		0	Interrupt When Index Equals Zero. If the Interrupt Enable Register IXEQZ bit is high, assertion of this bit enables generation of an interrupt for (a) subaddresses using indexed buffer mode when the INDX value decrements from 1 to 0, or (b) subaddresses using a circular buffer mode when the pre-determined number of messages has been transacted. If enabled, upon completion of command processing that results in index = 0, an IXEQZ interrupt is entered in the Pending Interrupt Register, output pin $\overline{INTMES}$ is asserted, and the interrupt is registered in the Interrupt Log.
14	IWA		0	Interrupt When Accessed. If the Interrupt Enable Register IWA bit is high, assertion of this bit enables interrupt generation when the subaddress receives any valid transmit command. If enabled, upon completion of command processing, an IWA interrupt is entered in the Pending Interrupt Register, output pin $\overline{INTMES}$ is asserted, and the interrupt is registered in the Interrupt Log.
13	-----		0	Not Used
12	MKBUSY		0	Make Busy. The host asserts the MKBUSY bit to respond with Busy status for commands to this transmit subaddress. This bit is an alternative to globally applying Busy status for all valid commands, enabled from the 1553 Status Bits Register. See that register description for additional information. When Busy is asserted, data words are not transmitted and the DPB bit does not toggle after message completion.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
11	DBAC		0 SR = 0	Descriptor Block Accessed. Internal device logic asserts the DBAC bit upon completion of message processing. The host may poll this bit to detect subaddress activity, instead of using host interrupts. This bit is reset to logic zero by $\overline{MR}$ master reset, SRST software reset or a read cycle to this memory address.
10	DPB		0 SR = 0	Data Pointer B. This status bit is maintained by the device and only applies in ping-pong buffer mode. This bit indicates the buffer to be used for the next occurring transmit command to this subaddress. When the DPB bit is logic 0, the next message will use Data Pointer A; when DPB is logic 1, the next message uses Data Pointer B. In ping-pong buffer mode, the bit is inverted after each error-free message completion. The DPB bit is not altered after messages ending in error, after illegal commands or after messages when the terminal responds with Busy status. This bit is reset to logic 0 by $\overline{MR}$ master reset or SRST software reset; therefore the first message received after either reset will use Buffer A. This bit is “don’t care” for indexed single-buffer mode or either circular buffer mode.
9	BCAST		0 SR = 0	Broadcast Received. The device sets this bit when a broadcast-transmit command is received for this subaddress. Because non-mode broadcast-transmit commands are always illegal, the assertion of this bit in the Control Word by the device indicates an illegal command was received. Terminal response varies, depending on whether or not illegal command detection applies (any bits set in Illegalization Table). This bit has no function if the BCSTINV bit is asserted in Configuration Register 1; in this case commands to RT address 31 are not recognized as valid by the device. This bit is reset to logic 0 by $\overline{MR}$ master reset or SRST software reset.
8	PPON		0	Ping-Pong Enable Acknowledge. This bit is controlled by the device and should not be written by the host. It only applies if PPEN bit 2 was initialized to logic one by the host after reset, enabling ping-pong buffer mode for this subaddress. The RT asserts this bit when it recognizes ping-pong is active for this subaddress. Before loading the transmit data buffer for this subaddress, the host can ask the RT to temporarily disable ping-pong by asserting STOPP bit 3. The RT acknowledges ping-pong is disabled by negating PPON. The host can safely load the buffer without data collision while PPON is negated. After buffer servicing, the host asks the RT to re-enable ping-pong by negating STOPP bit 3. The RT acknowledges ping-pong is re-enabled by asserting PPON. If PPEN bit 2 is high and PPON bit 8 is low when new commands arrive for this subaddress, ping-pong is disabled. Each new message transmits data from the same buffer, specified by DPB bit 10, and the DPB bit does not toggle after command completion.
7-4	CIR2ZN		0	Circular Mode 2 Zero Number. Used only in circular buffer mode 2, this 4-bit field is initialized with the number of trailing zeros in the initialized MIBA address. This is explained in Section 11.6, which fully describes circular buffer mode 2.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Function</th></tr>
<tr><td>3</td><td>STOPP</td><td></td><td>0</td><td>Stop Ping-Pong Request.
The host asserts this bit to suspend ping-pong buffering for this subaddress. The host resets this bit to ask the RT to re-enable ping-pong. The RT confirms recognition of ping-pong enable or disable status by writing PPON bit 8. Refer to later section describing ping-pong mode for more information.</td></tr>
<tr><td>2
1
0</td><td>PPEN
CIR2EN
CIR1EN</td><td></td><td>0
0
0</td><td>Ping-Pong, Circular Buffer Mode 2 or Circular Buffer Mode 1 Enable.
The PPEN, CIR2EN and CIR1EN bits are initialized by the host to select buffer mode. The table below summarizes how buffer mode selection is encoded.
In the case of ping-pong, the host initializes the PPEN bit to logic one after reset to enable ping-pong buffering for this subaddress. The host asserts STOPP bit 3 to ask the device to temporarily disable ping-pong. Negating the STOPP bit asks the device to re-enable ping-pong. The device confirms ping-pong enable or disable state changes by writing the PPON bit.
<table>
<tr><th>PPEN</th><th>CIR2EN</th><th>CIR1EN</th><th>Buffer Mode</th></tr>
<tr><td>1</td><td>Don’t Care</td><td>Don’t Care</td><td>Ping-Pong</td></tr>
<tr><td>0</td><td>1</td><td>Don’t Care</td><td>Circular Mode 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Circular Mode 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Indexed Single Buffer</td></tr>
</table>
</td></tr>
</table>

10.3. Data Buffer Options for Mode Code Commands

Data buffer options for mode code commands differ from options offered for subaddress commands. Mode commands cannot use either circular data buffer method, but may use double (ping-pong) buffering or single (indexed) buffering. Single message Index mode (INDX = 0) is suitable in many applications (see Section 11.4.1). An alternative called **Simplified Mode Command Processing** (SMCP) may be globally applied for all mode code commands (see Section 12.5).

To use single (indexed) buffer or double (ping-pong) buffer for mode commands, the SMCP bit in Configuration Register 1 is logic 0. The Control Word PPEN bit for each mode command determines whether ping-pong or indexed buffering is used.

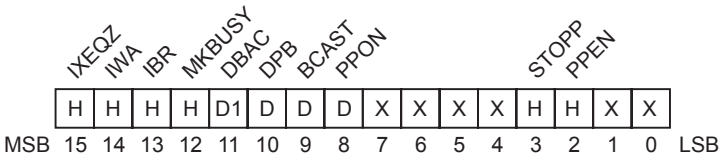
To use Simplified Mode Command Processing, the SMCP bit in Configuration Register 1 is set to logic 1. The Control Word PPEN bit for mode commands is “don’t care” (no longer specifies index or ping-pong buffer mode) because Simplified Mode Command Processing stores mode command data and message information words directly within each mode command’s redefined Descriptor Table block. When SMCP is enabled, mode code command descriptor blocks (in the Descriptor Table) do not contain data pointers to reserved buffers elsewhere in the shared RAM. Instead, each 4-word descriptor block itself contains the message information word, the time-tag word and the data word transacted for each mode command (for mode codes 16-31 decimal).

When Simplified Mode Command Processing is used, the range of active bits is reduced in each receive or transmit mode command Control Word. Interrupt control and response is not affected by the SMCP option. Simplified Mode Command Processing is fully presented in the later data sheet section entitled “Mode Code Commands.”

10.4. Receive Mode Command Control Word

Receive Mode Command Control Words apply when the command word T/$\overline{R}$ bit equals zero (receive) and the sub-address field has a value of 0 or 31 (0x1F). The descriptor Control Word defines terminal command response and interrupt behavior, and conveys activity status to the host. It is initialized by the host before terminal execution begins. Bits 8-11 cannot be written by the host; these bits are updated by the device during terminal execution, that is, when Configuration Register 1 STEX bit equals 1. The host can write bit 2 only when STEX equals zero; bits 3 and 12-15 can be written anytime. This register is cleared to 0x0000 by $\overline{MR}$ master reset. Software reset (SRST) clears just the DBAC, DPB and BCAST bits. **Following any read cycle to the Control Word address, the DBAC bit is reset.**

When single-message indexed buffering or ping-pong buffering is used instead of SMCP (Simplified Mode Code Processing), the receive mode Command Control Word looks like this:



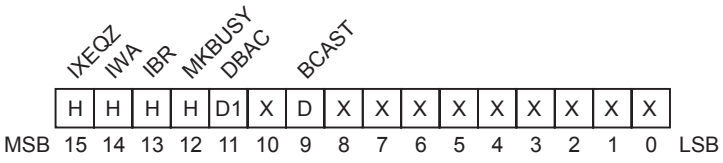
H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

When SMCP applies, the number of active mode Command Control Word bits is reduced:



H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
15	IXEQZ		0	Interrupt When Index Equals Zero. If the Interrupt Enable Register IXEQZ bit is high, assertion of this bit enables generation of an interrupt for mode code commands using indexed buffer mode when the INDX value decrements from 1 to 0. Upon completion of command processing that results in INDX = 0, when IXEQZ interrupts are enabled, an IXEQZ interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log.
14	IWA		0	Interrupt When Accessed. If the Interrupt Enable Register IWA bit is high, assertion of this bit enables interrupt generation at each instance of a valid mode code command. Upon completion of command processing, when IWA interrupts are enabled, an IWA interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log.

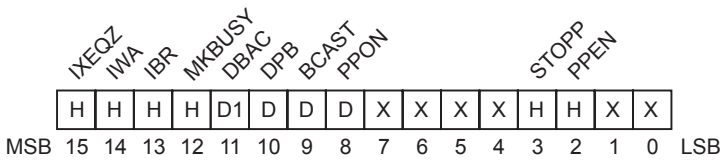
Bit No.	*Mnemonic*	*R/W*	*Reset*	*Function*
13	IBR		0	Interrupt Broadcast Received. If the Interrupt Enable Register IBR bit is high, assertion of this bit enables interrupt generation at each instance of a valid broadcast receive mode code command. Upon completion of command processing, when IBR interrupts are enabled, an IBR interrupt is entered in the Pending Interrupt Register, the $\overline{\text{INTMES}}$ output pin is asserted, and the interrupt is registered in the Interrupt Log. This bit has no function if the BCSTINV bit is high in Configuration Register 1. In this case, commands to RT address 31 are not recognized as valid by the device.
12	MKBUSY		0	Make Busy. The host asserts the MKBUSY bit to respond with Busy status for commands to this mode code. This bit is an alternative to globally applying Busy status for all valid commands, enabled from the 1553 Status Bits Register. See that register description for additional information. When Busy is asserted, mode data words received with MC16-MC31 are not stored and the DPB bit does not toggle after message completion.
11	DBAC		0 SR = 0	Descriptor Block Accessed. Internal device logic asserts the DBAC bit upon completion of message processing. The host may poll this bit to detect mode command activity, instead of using host interrupts. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset, SRST software reset or a read cycle to this memory address.
10	DPB		0 SR = 0	Data Pointer B. This status bit is maintained by the device and only applies for mode commands using ping-pong buffer mode. This bit indicates the buffer to be used for the next occurring mode command. When the DPB bit is logic 0, the next message will use Data Pointer A; when DPB is logic 1, the next message uses Data Pointer B. In ping-pong buffer mode, the bit is inverted after each error-free message completion. The DPB bit is not altered after messages ending in error, after illegal commands, or after messages when the terminal responds with Busy status. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset or SRST software reset; therefore the first message received after either reset will use Buffer A. This bit is “don’t care” for indexed single-buffer mode.
9	BCAST		0 SR = 0	Broadcast Received. Device logic sets this bit when a valid broadcast mode command is received having T/$\overline{\text{R}}$ bit = 0. This bit has no function if the BCSTINV bit is asserted in Configuration Register 1. In this case, RT address 31 commands are not recognized as valid by the HI-6120/21. This bit is reset to logic 0 by $\overline{\text{MR}}$ master reset or SRST software reset.

Bit No.	Mnemonic	R/W	Reset	Function
8	PPON		0	Ping-Pong Enable Acknowledge. This bit is read only and only applies for mode commands using ping-pong mode (PPEN bit 2 was initialized to logic 1 by the host after reset). The device asserts this bit when it recognizes ping-pong is active for this mode code. Before off-loading the receive data buffer for this mode code, the host can ask the device to temporarily disable ping-pong by asserting STOPP bit 3. The device acknowledges ping-pong is disabled by negating PPON. The host can safely load or off-load the buffer without data collision while PPON is negated. After buffer servicing, the host asks the device to re-enable ping-pong by negating STOPP bit 3. The device acknowledges ping-pong is re-enabled by asserting PPON. If PPEN bit 2 is high and PPON bit 8 is low when new commands arrive for this subaddress, ping-pong is disabled. Each new message overwrites existing data in the buffer specified by DPB bit 10, and the DPB bit does not toggle after command completion.
7-4	-----		0	Not Used
3	STOPP		0	Stop Ping-Pong Request. The host asserts this bit to suspend ping-pong buffering for this mode code. The host resets this bit to ask the device to re-enable ping-pong. The device confirms recognition of ping-pong enable or disable status by writing PPON bit 3.
2	PPEN		0	Ping-Pong Buffer Enable. The PPEN bit is initialized by the host to select buffer mode. If this bit is high, ping-pong buffering is selected. If this bit is low, indexed single buffering is selected. After reset, the host initializes this bit to logic 1 to enable ping-pong buffering for this mode code. The host asserts STOPP bit 3 to ask the device to temporarily disable ping-pong. Negating the STOPP bit asks the device to re-enable ping-pong. The device confirms ping-pong enable or disable state changes by writing the PPON bit.
1,0	-----		0	Not Used.

10.5. Transmit Mode Command Control Word

Transmit Mode Command Control Words apply when the command word T/$\overline{R}$ bit equals one (transmit) and the subaddress field has a value of 0 or 31 (0x1F). The descriptor Control Word defines terminal command response and interrupt behavior, and conveys activity status to the host. It is initialized by the host before terminal execution begins. Bits 8-11 cannot be written by the host; these bits are updated by the device during terminal execution, that is, when Configuration Register 1 STEX bit equals 1. The host can write bit 2 only when STEX equals zero; bits 3 and 12-15 can be written anytime. This register is cleared to 0x0000 by $\overline{MR}$ master reset. Software reset (SRST) clears just the DBAC, DPB and BCAST bits. **Following any read cycle to the Control Word address, the DBAC bit is reset.**

When single-message indexed buffering or ping-pong buffering is used instead of SMCP (Simplified Mode Code Processing), the transmit mode Command Control Word looks like this:



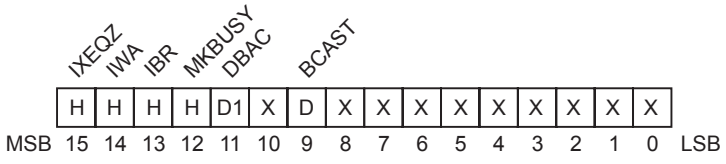
H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

When SMCP applies, the number of active mode Command Control Word bits is reduced:



H Bit maintained by host

D Bit maintained by device

D1 Bit set by device, reset by host read cycle

X Bit is not used, may be logic 0 or 1

NOTE: '*Reset*' refers to bit value following Master Reset ($\overline{MR}$). The bit value following software reset is unchanged unless specifically indicated by an "SR" value.

Bit No.	*Mnemonic*	*RW*	*Reset*	*Function*
15	IXEQZ		0	Interrupt When Index Equals Zero. If the Interrupt Enable Register IXEQZ bit is high, assertion of this bit enables generation of an interrupt for mode code commands using indexed buffer mode when the INDX value decrements from 1 to 0. Upon completion of command processing that results in INDX = 0, when IXEQZ interrupts are enabled, an IXEQZ interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log.
14	IWA		0	Interrupt When Accessed. If the Interrupt Enable Register IWA bit is high, assertion of this bit enables interrupt generation at each instance of a valid mode code command. Upon completion of command processing, when IWA interrupts are enabled, an IWA interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log.
13	IBR		0	Interrupt Broadcast Received. If the Interrupt Enable Register IBR bit is high, assertion of this bit enables interrupt generation at each instance of a valid broadcast transmit mode code command. Upon completion of command processing, when IBR interrupts are enabled, an IBR interrupt is entered in the Pending Interrupt Register, the $\overline{INTMES}$ output pin is asserted, and the interrupt is registered in the Interrupt Log. This bit has no function if the BCSTINV bit is high in Configuration Register 1. In this case, commands to RT address 31 are not recognized as valid by the device.

Bit No.	*Mnemonic*	*RW*	*Reset*	*Function*
12	MKBUSY		0	Make Busy. The host asserts the MKBUSY bit to respond with Busy status for commands to this mode code. This bit is an alternative to globally applying Busy status for all valid commands, enabled from the 1553 Status Bits Register. See that register description for additional information. When Busy is asserted, mode data words are not transmitted with MC16-MC31, and the DPB bit does not toggle after message completion. The MKBUSY bit is not heeded if set in the Control Word for mode code command MC8 “reset remote terminal”. For this command only, Busy is inhibited for the status response transmitted before the reset process begins.
11	DBAC		0 SR = 0	Descriptor Block Accessed. Internal device logic asserts the DBAC bit upon completion of message processing. The host may poll this bit to detect mode command activity, instead of using host interrupts. This bit is reset to logic 0 by $\overline{MR}$ master reset, SRST software reset or a read cycle to this memory address.
10	DPB		0 SR = 0	Data Pointer B. This status bit is maintained by the device and only applies for mode commands using ping-pong buffer mode. This bit indicates the buffer to be used for the next occurring mode command. When the DPB bit is logic 0, the next message will use Data Pointer A; when DPB is logic 1, the next message uses Data Pointer B. In ping-pong buffer mode, the bit is inverted after each error-free message completion. The DPB bit is not altered after messages ending in error, after illegal commands, or after messages when the terminal responds with Busy status. This bit is reset to logic 0 by $\overline{MR}$ master reset or SRST software reset; therefore the first message received after either reset will use Buffer A. This bit is “don’t care” for indexed single-buffer mode.
9	BCAST		0 SR = 0	Broadcast Received. Device logic sets this bit when a valid broadcast mode command is received having T/$\overline{R}$ bit = 1. This bit has no function if the BCSTINV bit is asserted in Configuration Register 1. In this case, RT address 31 commands are not recognized as valid by the HI-6120/21. This bit is reset to logic 0 by $\overline{MR}$ master reset or SRST software reset.
8	PPON		0	Ping-Pong Enable Acknowledge. This bit is read only and only applies for mode commands using ping-pong mode (PPEN bit 2 was initialized to logic 1 by the host after reset). The device asserts this bit when it recognizes ping-pong is active for this mode code. Before loading the transmit data buffer for this mode code, the host can ask the device to temporarily disable ping-pong by asserting STOPP bit 3. The device acknowledges ping-pong is disabled by negating PPON. The host can safely load or off-load the buffer without data collision while PPON is negated. After buffer servicing, the host asks the device to re-enable ping-pong by negating STOPP bit 3. The device acknowledges ping-pong is re-enabled by asserting PPON. If PPEN bit 2 is asserted and PPON bit 8 is negated when a new command arrives for this mode code, ping-pong disable handshake is in effect: The device applies single-buffer index mode using Data Pointer A or Data Pointer B, per DPB bit 10. The DPB bit does not toggle after command completion.

Bit No.	*Mnemonic*	*RW*	*Reset*	*Function*
7-4	-----		0	Not Used
3	STOPP		0	Stop Ping-Pong Request. The host asserts this bit to suspend ping-pong buffering for this mode code. The host resets this bit to ask the device to re-enable ping-pong. The device confirms recognition of ping-pong enable or disable status by writing PPON bit 3.
2	PPEN		0	Ping-Pong Buffer Enable. The PPEN bit is initialized by the host to select buffer mode. If this bit is high, ping-pong buffering is selected. If this bit is low, indexed single buffering is selected. After reset, the host initializes this bit to logic 1 to enable ping-pong buffering for this mode code. The host asserts STOPP bit 3 to ask the device to temporarily disable ping-pong. Negating the STOPP bit asks the device to re-enable ping-pong. The device confirms ping-pong enable or disable state changes by writing the PPON bit.
1,0	-----		0	Not Used.

11. MESSAGE DATA BUFFERS

The memory structures described up to this point comprise not more than 1K words of the lower memory address space. The remaining memory is allocated by the host for message data storage, to fulfill application requirements. This section describes the remaining data structures in shared RAM that control (and result from) command processing.

By initializing the Descriptor Table, the host allocates memory space for storing data for each subaddress used in the Remote Terminal application. Each legal Receive Subaddress and each legal Transmit Subaddress are usually assigned unique buffer memory spaces. (Exception: To comply with the requirements for MIL-STD-1553 data wrap-around, it is convenient to assign the data wrap-around subaddress to use the same buffer space for both receive and transmit commands.)

As an option, data from broadcast receive commands can be stored separately from data resulting from non-broadcast receive commands. Each subaddress buffer can use any of four data storage methods offered.

Subaddress (non-mode) commands are transacted with one to 32 data words. These are stored in a data buffer in shared RAM. For receive commands, the device stores data received during message processing in the shared RAM buffer. Later, the host retrieves these data words from the buffer. In the case of transmit commands, the host has previously stored transmit data words in the transmit subaddress buffer. The device retrieves these data words for transmission while processing the transmit command.

For each complete message processed, the message data stored in the buffer is comprised of these elements:

1. Message Information Word.
2. Time-Tag Word.
3. One to 32 Data Words transmitted or received during message transaction (except no data word for mode code commands 0 - 15 decimal).

The Message Information word and Time-Tag word are generated by the device and stored in assigned buffer space to aid the host in further message processing. The Message Information word contains message type, word count and message error information. The 16-bit Time-Tag word contains the value in the device internal Time-Tag counter when the command is validated.

The host initializes the Descriptor Table entry for each subaddress or mode command to select one of four data buffering methods.

1. **Indexed (Single Buffer) Method (see 11.4).**

   A predetermined number of messages (N) is transacted using a single data buffer in shared RAM. Several host interrupt options are offered, including host interrupt when all N messages are successfully completed. This method also supports single-message mode when N is purposely initialized to zero.

2. **Double (or Ping-Pong) Buffer Method (see 11.3).**

   Successive messages alternate between two 34-word data buffers in shared RAM. Several host interrupt options are offered.

3. **Circular Buffer Mode 1 (see 11.5).**

   Buffer boundaries determine when the bulk transfer is complete. Message information and time-tag words are stored in the same buffer with data words. Several host interrupt options are offered, including host interrupt when the allocated data buffer is full.

4. **Circular Buffer Mode 2 (see 11.6).**

   The number of messages transacted defines bulk transfer progress. Message data words are stored contiguously in one buffer while message information and time-tag words are stored in a separate buffer. Several host interrupt options are offered, including host interrupt when all N messages are completed.

The data buffer options are summarized in Table 8.

Simplified Mode Command Processing.

This is a global option that applies for all mode code commands, when enabled. Mode commands have either one data word, or no data word. Instead of using data buffers for storing this limited mode command data, the message data is stored directly within the Descriptor Table. This option for mode commands is described in the section called “Mode Command Processing.”

Broadcast Data Separation

When the NOTICE2 option is enabled, data words resulting from broadcast receive commands will be stored separately from data resulting from non-broadcast receive commands when using indexed or ping-pong buffer modes. When NOTICE2 applies, all subaddresses using indexed or ping-pong modes must have an assigned 34-word broadcast data buffer in addition to the primary buffers listed above. Broadcast data segregation cannot be done using either circular buffer mode.

Table 8. Summary of Data Buffer Modes.

Buffer Mode	Data Buffer(s) Number and Size	Message Info Word	Suitable for Mode Codes?	Primary Application
Indexed	One. Host defines size for N messages	Stored in same buffer as data	Yes, only single message mode	For transacting N (multiple) messages with optional host interrupt when done
Ping-Pong	Two 34-word buffers, one message each	Stored in same buffer as data	Yes	For transacting single messages, alternating between A and B buffers
Circular 1	One. Host defines size for N words	Stored in same buffer as data	No	For transacting messages until buffer is full / empty, optional interrupt when done
Circular 2	One. Host defines size for N messages, plus Msg Info Block	Stored in separate buffer (Msg info block)	No	For transacting N (multiple) messages with optional host interrupt when done. Data buffer holds contiguous pure data.

11.1. Subaddress Message Information Words

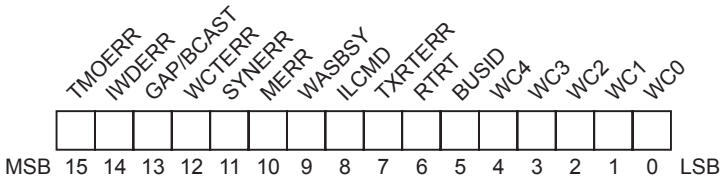
11.1.1. Receive Subaddress Command

For receive subaddress commands, the device stores the received data words plus two additional words. The device adds a receive subaddress Message Information Word and a Time-Tag Word to the received data words. The device stores the Message Information and Time-Tag words ahead of the data words associated with the receive command, as shown below. If message error occurs, the RT stores only the receive subaddress Message Information Word and Time-Tag Word. Once a message error is detected, the device sets the MERR bit in the receive subaddress Message Information word. When this occurs, all data words are considered invalid. Whenever the receive subaddress Message Information Word MERR bit is set, the host should disregard the record's data word(s).

Here is an example data structure for a 3-word receive command. Notice that the receive subaddress Data Pointer points to the data structure starting address, not the first data word. The data pointer is located in the receive subaddress command's Descriptor Block, fully described later:

		Data Buffer Hex Address	Word Description	Device Writes Word ...
Data pointer equals 0x0500	→	0x0500	Message Information Word	After message completion
		0x0501	Time-Tag Word	" " "
		0x0502	Data Word 1	After message completion (See **Note**)
		0x0503	Data Word 2	" " " " "
		0x0504	Data Word 3	" " " " "

Note: The data words are written after message completion when Configuration Register 2 TRXDB is 1, otherwise written when received.



The following bits comprise the receive subaddress Message Information Word:

Bit No.	*Mnemonic*	*Function*
15	TMOERR	Time-Out Error. This bit is asserted for RT-RT receive messages when the transmitting terminal fails to start its status word and data transmission before time-out occurs, per TOSEL0-1 bits in Configuration Register 2.
14	IWDERR	Invalid Word Error. Assertion of this bit indicates Manchester error or parity error was observed in a received data word.
13	GAP/ BCAST	Gap Error / Broadcast Flag. When “Configuration Register 2 (0x0001)” bit 3 is “0”, this bit is a **Gap Error flag**. Assertion of this bit indicates bus activity was detected immediately after the last expected receive data word or that a gap occurred before all expected data words were received. When “Configuration Register 2 (0x0001)” bit 3 is “1”, this bit is a **Broadcast flag**, asserted when the received message was broadcast.
12	WCTERR	Word Count Error. This bit is asserted if command is received with less data words than the command word specifies. For example, a receive command for three data words is received with two contiguous data words.
11	SYNERR	Sync Error. This bit is asserted when an incorrect (command/status) sync type occurs in received data words.
10	MERR	Message Error. This bit is asserted when message error status change occurs during command processing. See bits 7 and 11-15 for details.
9	WASBSY	Was Busy. This bit is asserted when the terminal responds to the receive command with BUSY status, due to global BUSY bit set in 1553 Status Bits Register, or command-specific MKBUSY bit set in the descriptor table Control Word. Received data words were buffered normally.
8	ILCMD	Illegal Command Received. This bit is asserted when the Illegalization Table bit corresponding to the received command is logic 1. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. See section entitled Illegalization Table for further information.

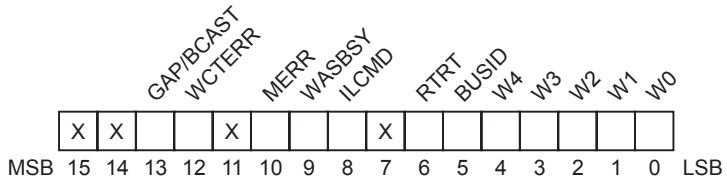
Bit No.	*Mnemonic*	*Function*
7	TXRTERR	RT-RT Transmit Remote Terminal Error. This bit is set when the terminal decodes a valid RT-RT receive command, but one of four potential errors is detected in the second command word, CW2: (1) CW2 is addressed to broadcast address RT31. (2) the CW2 T/$\overline{R}$ bit equals 0, (3) the CW2 subaddress is a mode command indicator, 00000 or 11111, or (4) CW2 has same non-broadcast terminal address as receive command word CW1. The TXRTERR bit is also set when status word received from the transmitting terminal is invalid (e.g., parity error) or bits 15:11 in the status word reflect the wrong RT address (does not match CW2).
6	RTRT	Remote Terminal to Remote Terminal Transfer. Assertion of this bit indicates the receive command was an error-free RT-to-RT transfer.
5	BUSID	Bus Identification. If this bit equals zero, message was transacted on Bus A. If bit equals one, it was transacted on Bus B.
4-0	WC4:0	Word Count. This 5-bit field contains the word count extracted from the command word. Zero indicates 32 words.

11.1.2. Transmit Subaddress Command

The external host is responsible for organizing the data packet (i.e., storing N data words) in shared RAM and initializing the applicable data pointer. The host must allocate two memory locations at the starting address of the data record for device storage of the transmit subaddress Message Information Word and Time-Tag Word.

Here is an example data structure for a 3-word transmit command. Notice that the Data Pointer points to the data structure starting address, not the first data word. The data pointer is located in the transmit subaddress command's Descriptor Block.

		Data Buffer Hex Address	**Word Description**	**Word is Written By ...**
Data pointer equals 0x0500	→	0x0500	Message Information Word	Device, after message completion
		0x0501	Time-Tag Word	" " " "
		0x0502	Data Word 1	Host, prior to terminal's data transmit
		0x0503	Data Word 2	" " " " " "
		0x0504	Data Word 3	" " " " " "



The following bits comprise the transmit subaddress Message Information Word.

Bit No.	*Mnemonic*	*Function*
15,14	-----	Not Used.
13	GAP/ BCAST	Gap Error / Broadcast Flag. When “Configuration Register 2 (0x0001)” bit 3 is 0, this bit is a **Gap Error flag**. Assertion of this bit indicates bus activity was detected immediately after the transmit command word, when a gap was expected. When “Configuration Register 2 (0x0001)” bit 3 is 0, this bit is a **Broadcast flag**, asserted when the received message was broadcast.
12	WCTERR	Word Count Error. This bit is asserted if command is received with unexpected data word(s).
11	-----	Not Used.
10	MERR	Message Error. This bit is asserted when message error status change occurs during command processing. See bits 12 and 13 for details.
9	WASBSY	Was Busy Status. This bit is asserted when the terminal responds to the transmit command with BUSY status, due to global BUSY bit set in 1553 Status Bits Register, or command-specific MK-BUSY bit set in the descriptor table Control Word. No data words were transmitted.
8	ILCMD	Illegal Command Received. This bit is asserted when the Illegalization Table bit corresponding to the received command equals one. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. See section entitled Illegalization Table for further information.
7	-----	Not Used.
6	RTRT	Remote Terminal to Remote Terminal Transfer. Assertion of this bit indicates the transmit command was an error-free RT-to-RT transfer.
5	BUSID	Bus Identification. If this bit equals zero, message was transacted on Bus A. If bit equals one, it was transacted on Bus B.
4-0	WC4:0	Word Count. This 5-bit field contains the word count extracted from the command word. Zero indicates 32 words.

11.2. Mode Command Message Information Words

Mode command data structures in shared RAM are similar to those for subaddresses. Mode codes 0 through 15 (0x0F) do not have an associated data word, so data structures for these mode code values have just a Message Information Word and Time-Tag Word. The Message Information Word is stored at the memory address specified by the descriptor table Data Pointer. Mode codes 16 through 31 (0x10 through 0x1F) have one associated data word. The Message Information Word is stored at the memory address specified by the descriptor table Data Pointer, and the Time-Tag Word is stored in the following location. The data word is stored at the memory address specified by the Data Pointer plus two locations.

11.2.1. Receive Mode Command

The receive mode command data structure contains a Message Information Word, a Time-Tag Word and may contain one Data Word. If a receive mode command has a data word, the device may apply the data as defined by MIL-STD-1553, plus store the received single mode data word at the address specified by the Data Pointer, plus two locations. Refer to data sheet section entitled “Mode Command Action Summary”.

Here is an example data structure for a receive mode command with data (mode code values 0x10 through 0x1F). Notice that the Data Pointer points to the data structure starting address, not the mode data word. The data pointer is located in the receive mode command’s Descriptor Block, fully described later:

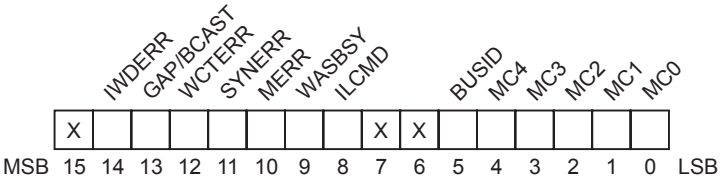
		Data Buffer Hex Address	Word Description	Word is Written By ...
Data pointer equals 0x0500	→	0x0500	Message Information Word	Device, after message completion
		0x0501	Time-Tag Word	“ “ “ “
		0x0502	Mode Data Word	“ “ “ “

Three receive mode commands with data are not defined under MIL-STD-1553B. These are MC16, MC18 and MC19 (mode codes 0x10, 0x12 and 0x13 respectively). However the device responds “in form” if illegal command detection is not used (corresponding bits in Illegalization Table are logic 0) **and** the UMCINV bit in Configuration Register 1 is logic 0.

For mode code commands without data, the data structure contains only the Message Information Word and Time-Tag Word.

Here is an example data structure for a receive mode command without data (mode code values 0x00 through 0x0F). Note: None of these receive mode commands are defined under MIL-STD-1553B but the device responds “in form” if illegal command detection is not used (corresponding bits in Illegalization Table are logic 0) and the UMCINV bit in Configuration Register 1 is logic 0. Notice that the data pointer points to the data structure starting address, the message information word. The data pointer is located in the receive mode command’s Descriptor Block, fully described later:

		Data Buffer Hex Address	Word Description	Word is Written By ...
Data pointer equals 0x0500	→	0x0500	Message Information Word	Device, after message completion
		0x0501	Time-Tag Word	“ “ “ “



The following bits comprise the receive mode Message Information Word:

Bit No.	*Mnemonic*	*Function*
15	-----	Not Used.
14	IWDERR	Invalid Word Error. Assertion of this bit indicates Manchester error or parity error was observed in a received data word.

Bit No.	*Mnemonic*	*Function*
13	GAP/ BCAST	Gap Error / Broadcast Flag. When “Configuration Register 2 (0x0001)” bit 3 is 0, this bit is a **Gap Error flag**. Assertion of this bit indicates bus activity was detected immediately after a received mode data word or that a gap occurred before the data word was received. When “Configuration Register 2 (0x0001)” bit 3 is 0, this bit is a **Broadcast flag**, asserted when the received message was broadcast.
12	WCTERR	Word Count Error This bit is asserted if the command is received without expected mode data word, or with extra word.
11	SYNERR	Sync Error. This bit is asserted when incorrect (command/status) sync type occurs in received mode data word.
10	MERR	Message Error. This bit is asserted when message error status change occurs during command processing. See bits 11- 14 for details.
9	WASBSY	Was Busy Status. This bit is asserted when the terminal responds to the mode command with BUSY status, due to global BUSY bit set in 1553 Status Bits Register, or command-specific MKBUSY bit set in the descriptor table Control Word.
8	ILCMD	Illegal Command Received. This bit is asserted when the Illegalization Table bit corresponding to the received command equals one. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. See section entitled Illegalization Table for further information.
7,6	-----	Not Used.
5	BUSID	Bus Identification. If this bit equals zero, message was transacted on Bus A. If bit equals one, it was transacted on Bus B.
4-0	MC4:0	Mode Code. This 5-bit field contains the mode code extracted from the command word.

11.2.2. Transmit Mode Command

The transmit mode command data structure contains a Message Information Word, a Time-Tag word and may contain one Data Word. For mode commands with associated data word (mode codes 16-31 decimal) the host is responsible for loading the Mode Command Data Table before transmit mode commands are received (e.g., Transmit Vector Word mode code). Two mode codes have internally generated data words: MC18 “Transmit Last Command” and MC19 “Transmit BIT Word”. For these, the device automatically transmits the data word then copies the transmitted data value to the stored data structure.

Here is an example data structure for a transmit mode command with data (mode code values 0x10 through 0x1F). This applies to MC16 “Transmit Vector Word”. Notice that the data pointer points to the data structure starting address,

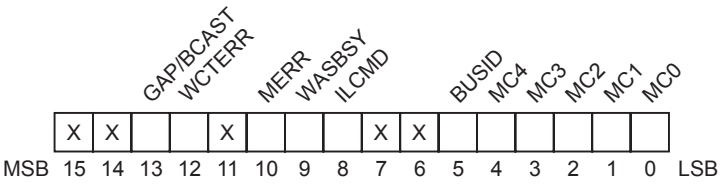
not the mode data word. The data pointer is located in the transmit mode command's Descriptor Block, fully described later:

		Data Buffer Hex Address	Word Description	Word is Written By ...
Data pointer equals 0x0500	→	0x0500	Message Information Word	Device, after message completion
		0x0501	Time-Tag Word	" " " "
		0x0502	Mode Data Word	Host, prior to terminal's data transmit (except MC18, MC19 are written by the device after completion)

Three transmit mode commands with data are not defined under MIL-STD-1553B. These are MC17, MC20 and MC21 (mode codes 0x11, 0x14 and 0x15 respectively). However the device responds "in form" if illegal command detection is not used (corresponding bits in Illegalization Table are logic 0) and the UMCINV bit in Configuration Register 1 is logic 0.

For mode code commands without data, the data structure contains only the Message Information Word and Time-Tag Word. Here is an example data structure for a transmit mode command without data (mode code values 0x00 through 0x0F). Again, the data pointer points to the data structure starting address. The data pointer is located in the transmit mode command's Descriptor Block, fully described later:

		Data Buffer Hex Address	Word Description	Word is Written By ...
Data pointer equals 0x0500	→	0x0500	Message Information Word	Device, after message completion
		0x0501	Time-Tag Word	" " " "



The following bits comprise the mode transmit Message Information Word:

Bit No.	*Mnemonic*	*Function*
15,14	-----	Not Used.
13	GAP/ BCAST	Gap Error / Broadcast Flag. When "Configuration Register 2 (0x0001)" bit 3 is 0, this bit is a **Gap Error flag**. This bit is high when bus activity was detected immediately after the mode command word, when a gap was expected. When "Configuration Register 2 (0x0001)" bit 3 is 0, this bit is a **Broadcast flag**, asserted when the received message was broadcast.
12	WCTERR	Word Count Error This bit is asserted if command is received with unexpected data word(s).
11	-----	Not Used.

Bit No.	*Mnemonic*	*Function*
10	MERR	Message Error. This bit is asserted when message error status change occurs during command processing. See bits 12-13 for details.
9	WASBSY	Was Busy Status. This bit is asserted when the terminal responds to the mode command with BUSY status, due to global BUSY bit set in 1553 Status Bits Register, or command-specific MKBUSY bit set in the descriptor table Control Word. No mode data word was transmitted.
8	ILCMD	Illegal Command Received. This bit is asserted when the Illegalization Table bit corresponding to the received command is logic 1. The Illegalization Table should only contain nonzero values when “illegal command detection” is being applied. See section entitled Illegalization Table for further information.
7,6	-----	Not Used.
5	BUSID	Bus Identification. If this bit equals zero, message was transacted on Bus A. If bit equals one, it was transacted on Bus B.
4-0	MC4:0	Mode Code. This 5-bit field contains the mode code extracted from the command word.

11.3. Ping-Pong Data Buffering

11.3.1. Double Buffered (Ping-Pong) Mode

Ping-pong buffer mode is a method for storing message and time-tag information and data associated with messages. Each unique MIL-STD-1553 subaddress and mode code is assigned a pair of data buffers for transmit commands and a pair of data buffers for receive commands. The device retrieves buffer data for transmit commands, or stores buffer data for receive commands. During ping-pong operation, the device alternates message storage between Data Buffer A and Data Buffer B, on a message-by-message basis.

When a subaddress or mode command uses ping-pong data buffer mode, its 4-word descriptor block in the Descriptor Table is defined as follows:

Descriptor Word 1	Control Word
Descriptor Word 2	Data Pointer A
Descriptor Word 3	Data Pointer B
Descriptor Word 4	Broadcast Data Pointer

If Descriptor Word 1 is stored at memory address N, Descriptor Word 2 is stored at address N+1, and the other two words are stored at addresses N+2 and N+3.

Prior to starting terminal operation, enable ping-pong buffering for any subaddress (or mode code) by asserting the PPEN bit and negating the STOPP bit in the descriptor Control Word. When the device detects ping-pong is selected (PPEN = 1) and enabled (STOPP = 0), it asserts the Control Word PPON bit to confirm ping-pong is active.

During ping-pong operation, the RT determines the active data buffer at the beginning of message processing. The Control Word DPB bit indicates the data pointer to be used by the next command. DPB equals logic 0 means Data Pointer A is used next; DPB equals logic 1 means Data Pointer B is used next. For ping-pong, Data Pointers A and B are static values pointing to the first address in each buffer. At the conclusion of error-free message processing, the Control Word DPB bit is inverted so the next command “ping-pongs” to the other data buffer. Each new message to the subaddress or mode code overwrites message data and information words written previously. To assure data integrity, the DPB pointer should only toggle after completion of error-free messages. To cover the full set of conditions, **set DPBTOFF bit 1 described in “Configuration Register 2 (0x0001)” on page 24**. When option bit DPBTOFF = 1, DPB pointer toggle is prevented after incomplete messages, illegal commands, and messages resulting in BUSY or MESSAGE ERROR status. (When option bit DPBTOFF = 0, the illegal and BUSY cases still cause DPB pointer toggle.)

Please note that a subaddress may contain both legal and illegal word counts. When DPBTOFF = 1, DPB pointer toggle only occurs for the expected (legal) word count(s).

The primary benefit of using the DPBTOFF = 1 option is always knowing where to find the most-recent valid data. When DPBTOFF = 1, the complemented DPB pointer always indicates the last-transacted “good” data set. For example, if DPB is logic 0, the last successful message used Data Buffer B.

(**Exception:** immediately following Master Reset, the entire memory range is cleared to zero, so neither buffer contains message data. After reset, the host typically initializes outgoing data for the first message occurring on each transmit subaddress, Buffer A. The Message Information and Time Tag Words will read 0x0000 until the first message is transacted. After reset, the first-used Buffer A for each receive subaddress will contain 0x0000 for the Message Information and Time Tag Words and all data locations, until the first message is transacted).

Figure 10 is a general illustration of ping-pong buffer mode. Figure 11 shows a specific example.

11.3.2. Ping-Pong Enable / Disable Handshake

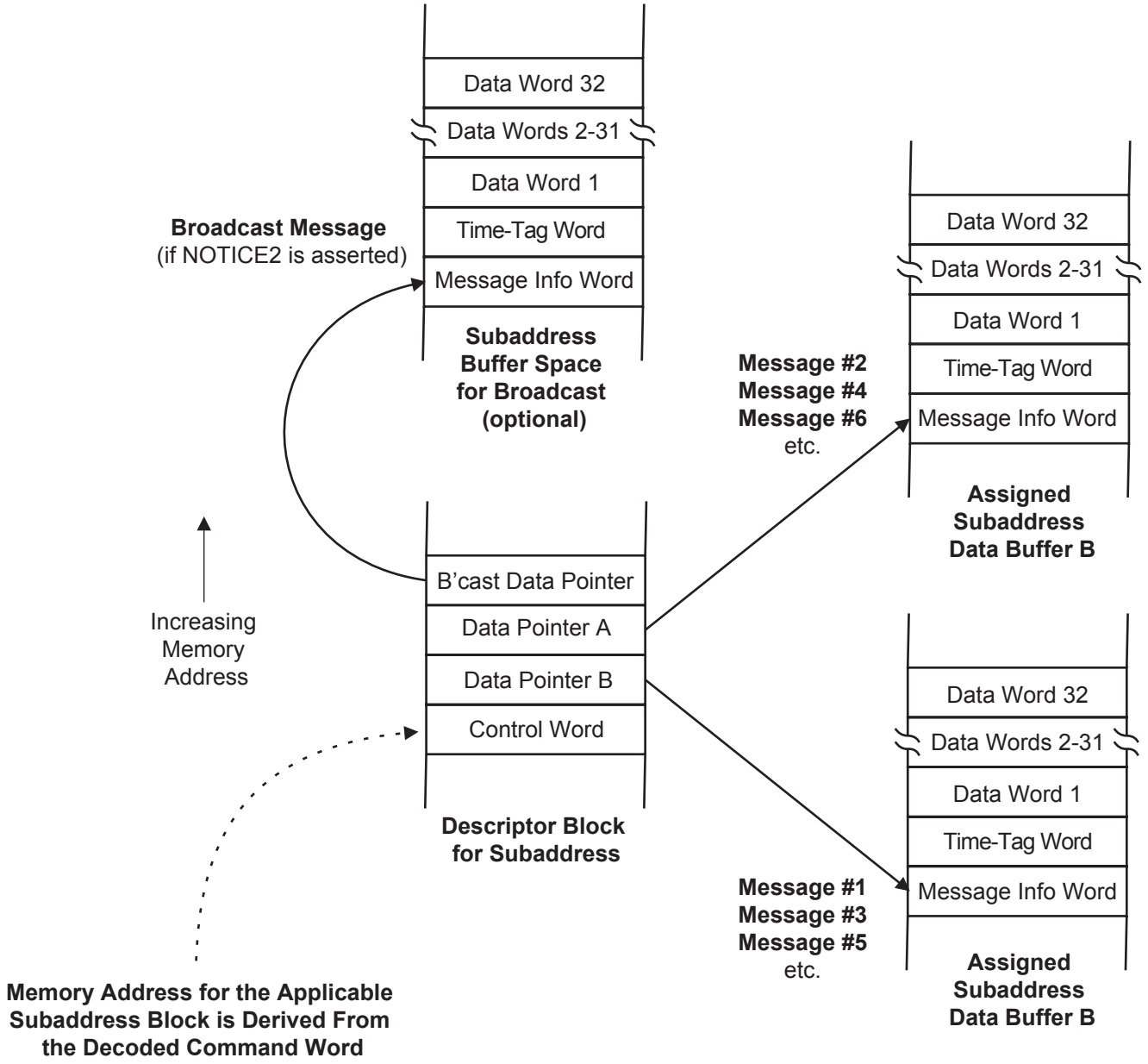
Because ping-pong messages and host buffer servicing are asynchronous, there is potential for “data collision”. Here is a data collision example: The host reads data from an earlier message while the device simultaneously writes new message data to the same buffer. The host reads a mix of new and old message data. Collisions can occur for both transmit and receive messages.

A handshake scheme lets the external host asynchronously service ping-pong data buffers without data collision. To off-load or load a subaddress (or mode code) buffer, the application software performs the following sequence:

a. Host asserts the Control Word STOPP bit to suspend ping-pong operation for the subaddress. When the device recognizes STOPP bit assertion, it negates the PPON bit to acknowledge ping-pong is disabled. While PPON remains low, the last written (or read) data buffer is protected against device updates. During this time, new messages use the active buffer indicated by the Control Word DPA bit. Recurring messages repeatedly use the same buffer until ping-pong resumes.

b. Host services the last-used data buffer. If the Control Word DPB bit equals logic 1, the last command used Buffer A. The host application software off-loads or loads inactive Buffer A while the remote terminal uses active Buffer B for new message(s). If the DPB bit equals logic 0, the last command used Buffer B. The host application software off-loads or loads inactive Buffer B while the remote terminal uses active Buffer A for any new messages. Each new receive message overwrites buffer contents from the last receive message. To avoid possible data loss, host buffer servicing should be timed for completion before a second message can occur.

c. Host negates the Control Word STOPP bit to resume ping-pong operation for the subaddress. When the RT recognizes the STOPP bit is reset, it sets the PPON bit to acknowledge ping-pong is again active. As long as PPON remains set, the device alternates between data buffers A and B for new messages.



Message processing alternates between Data Buffers A and B. Upon sucessful message completion, the DPB bit in Descriptor Control Word is updated so next message uses other buffer. Buffers are overwritten every other message.

Separate buffer for broadcast messages is optional. There is no alternate buffer for successive broadcast messages.

Figure 10. Illustration of Ping-Pong Buffer Mode

11.3.3. Broadcast Message Handling in Ping-Pong Mode

For MIL-STD-1553B Notice II compliance, a remote terminal should be capable of storing data from broadcast messages separately from non-broadcast message data. Some applications may not include this requirement. The standard does not stipulate where data separation should occur (e.g., within the RT or within the external host) so the device provides alternative strategies.

When the NOTICE2 bit in Configuration Register 1 is 1 and the BCSTINV bit is 0, ping-pong mode subaddresses (or mode codes) will buffer data words from broadcast and non-broadcast messages separately. Broadcast message information and data are stored in the broadcast data buffer; non-broadcast message information and data are stored in ping-pong buffers A and B. Since there is just one broadcast data buffer, the NOTICE2 option treats broadcast messages as exceptions to normal ping-pong mode. When using the NOTICE2 option, broadcast data buffer servicing should have high priority, because a closely following broadcast message will overwrite the broadcast buffer.

Every mode command and subaddress (including transmit subaddresses) must have an assigned valid broadcast data pointer when NOTICE2 is asserted. When the NOTICE2 bit in Configuration Register 1 is 1 and the BCSTINV bit is 0, reception of a broadcast-transmit message updates the Message Information and Time-Tag Words for the assigned broadcast buffer, but no data is transmitted on the bus. Since broadcast-transmit is not allowed, multiple transmit subaddresses may share a common “bit bucket” broadcast buffer. A two word buffer is sufficient for storing the MIW and Time-Tag Word.

When using ping-pong mode, there are two ways to handle broadcast messages, when broadcast is enabled:

Option 1 for Ping-Pong Mode Broadcast Messages:

This option isolates broadcast message information in the broadcast data buffer. If the descriptor Control Word IBR bit and Interrupt Enable Register IBR bit are both set, reception of broadcast messages generates an INTMES host interrupt. To prevent data loss, the broadcast data buffer must be serviced before the next broadcast message occurs. Broadcast messages do not affect non-broadcast message ping-pong; the Control Word DPB bit does not toggle after broadcast message completion.

Option 1 Setup: At initialization, host asserts the NOTICE2 bit in Configuration Register 1 and sets the IBR (Interrupt Broadcast Received) bit in descriptor Control Word(s). The IBR bit is asserted in the Interrupt Enable Register.

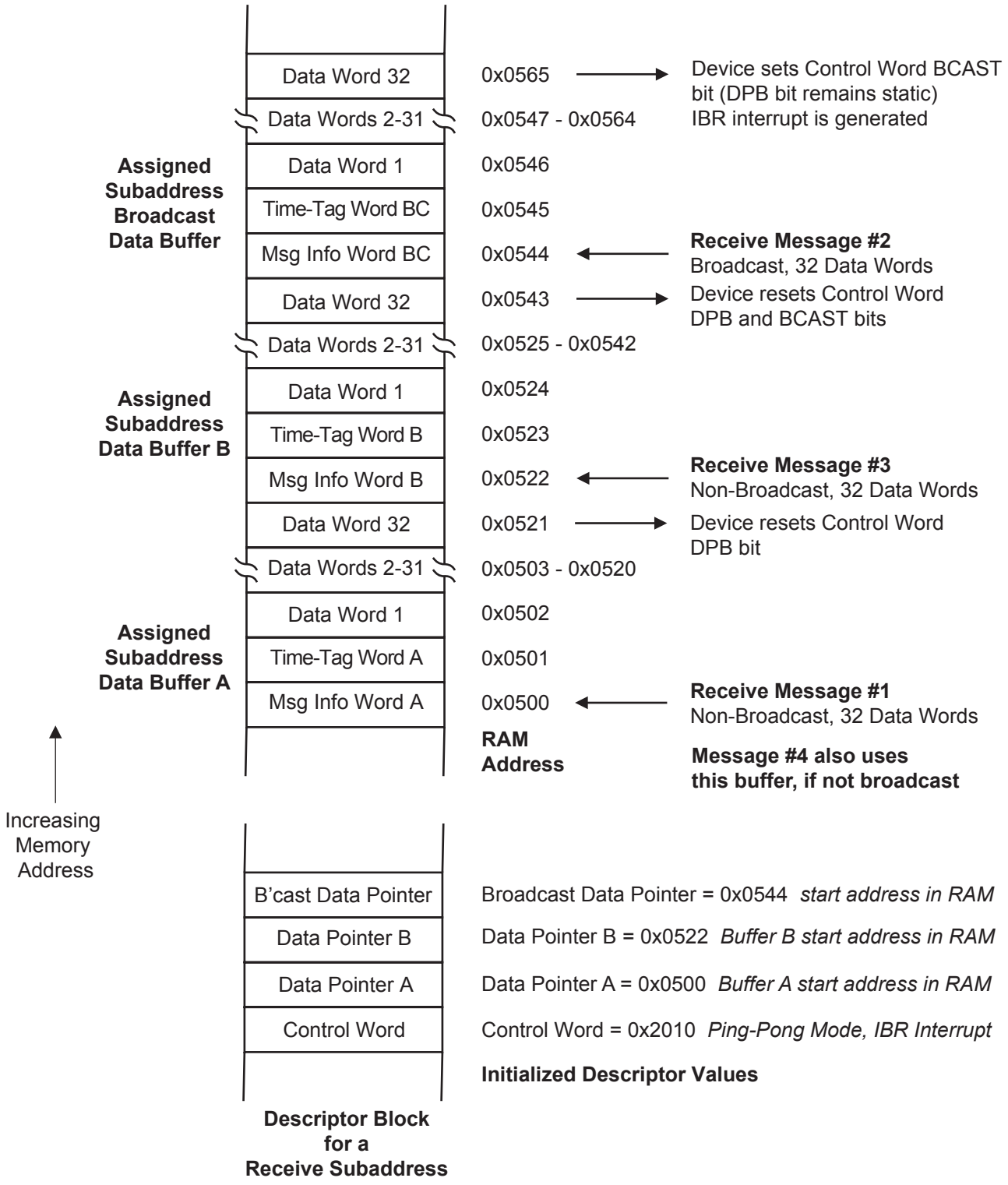
When a broadcast command is received, message information and data is stored in the broadcast data buffer and an $\overline{\text{INTMES}}$ interrupt is generated. The host must read the Interrupt Log to determine the originating subaddress (or mode code), then service the broadcast data buffer for that subaddress (or mode code) before another broadcast message to the same subaddress (or mode code) arrives.

Option 2 for Ping-Pong Mode Broadcast Messages:

The second alternative stores both broadcast and non-broadcast message information in the ping-pong data buffers A and B. IWA interrupts can signal arrival of any new message. The RT handles broadcast messages just like non-broadcast messages, except the Message Information Word BCAST bit is asserted to identify broadcast messages during host buffer servicing. All messages toggle the Control Word DPB bit in message post-processing. For Notice II compliance, separation of broadcast and non-broadcast data occurs within the host.

Option 2 Setup: At initialization, host negates the NOTICE2 bit in Configuration Register 1. If IWA interrupts are used, the host asserts the descriptor Control Word IWA (Interrupt When Accessed) bit 14 and the corresponding bit is asserted in the Interrupt Enable Register. Using this option, the IBR interrupt is probably not used.

The host typically services the ping-pong data buffers A and B whenever a message is transacted. Using the setup above, this occurs whenever the subaddress IWA interrupt generates an $\overline{\text{INTMES}}$ interrupt output for the host. The host must read the Interrupt Log to determine the originating subaddress or mode code. The applicable data buffer is indicated by the DPB bit in the Receive Control Word. The Message Information Word BCAST bit is asserted if the message was broadcast.



Following reset (which resets Control Word DPB bit), the subaddress transacts 4 commands of 32 data words each. The NOTICE 2 option is enabled so the device segregates data from broadcast and non-broadcast messages. Message #2 is a broadcast command, while the other three messages are non-broadcast. Notice that the broadcast message does not affect DPB bit, but the following message resets BCAST bit. The interspersed broadcast command does not affect alternation between Buffer A and Buffer B.

Figure 11. Ping-Pong Buffer Mode Example for a Receive Subaddress

11.4. Indexed Data Buffer Mode

Also called “single buffer mode”, indexed buffering is one method for storing message and time-tag information and data associated with messages. Buffer mode is selected for each subaddress or mode code in the Descriptor Table Control Words. Indexed mode is enabled when Control Word PPEN, CIR1EN and CIR2EN bits are all zero.

When a subaddress or mode command uses the indexed data buffer mode, its 4-word descriptor block in the Descriptor Table is defined as follows:

Descriptor Word 1	Control Word
Descriptor Word 2	Data Pointer A
Descriptor Word 3	INDX Index Word
Descriptor Word 4	Broadcast Data Pointer

If Descriptor Word 1 is stored at memory address N, Descriptor Word 2 is stored at address N+1, and the other two words are stored at addresses N+2 and N+3.

As the name implies, all message information and data is stored in a single buffer, indexed by descriptor word Data Pointer A. The descriptor Control Word DPB bit is “don’t care”. The host initializes the desired message count in descriptor INDX word. During message processing, the device retrieves or stores data words from the address specified by descriptor Data Pointer A, automatically incrementing the pointer address as words are read or stored. Data Pointer A is updated during command post-processing with the current buffer address unless the message index count in descriptor INDX (word 3 of descriptor block) decrements to zero upon completion of the message. Figure 12 is a general illustration of indexed single buffer mode. Figure 13 shows a specific example.

To set up a terminal subaddress to buffer multiple messages, the host writes the desired index count (INDX) to subaddress descriptor word 3. The initial INDX value ranges from zero to 3FF hex (1023) messages. The device decrements the INDX count each time an error-free message is transacted, and the data pointer is updated to the first memory address to be used for the next message. If INDX decrements from one to zero and Control Word IXEQZ bit 15 is asserted, the IXEQZ bit is set in the Interrupt Pending Register. If the corresponding bit in the Interrupt Enable Register is asserted, an $\overline{\text{INTMES}}$ interrupt is generated when INDX decrements from one to zero.

INDX counter decrement does not occur if the command was illegalized or if INDX already equals zero. Once INDX equals zero, further commands will overwrite the last-written data buffer block and the data pointer value is not updated after successful message completion.

When using Index Mode with a non-zero INDX value, the host must remember the initial Data Pointer A address. The Data Pointer A word is not automatically re-initialized to the buffer start address when INDX decrements from 1 to 0.

11.4.1. Single Message Mode

When Index Mode is initialized with an INDX value of zero, the subaddress or mode code is operating in “Single Message Mode”. Here, the same data block is repeatedly over-read (for transmit data) or overwritten (for receive or broadcast data). The DPA pointer is not updated at the end of each message. The chief advantage of single message mode is simplicity. In comparison to other data buffering options, the single message buffer uses an absolute minimum amount of memory space. The IXEQZ interrupt cannot be used for this scheme (INDX is always zero) but IWA interrupts may be used. Single message mode is best suited to synchronous data transfer where the host processor can reliably read or write new message data prior to the start of the next message to the same subaddress or mode code.

11.4.2. Broadcast Message Handling in Index Mode

For MIL-STD-1553B Notice II compliance, a remote terminal should be capable of storing data from broadcast messages separately from non-broadcast message data. Some applications may not include this requirement. The standard does not stipulate where data separation should occur (e.g., within the RT or within the external host) so the device supports alternative strategies.

When the NOTICE2 bit is logic 1 in Configuration Register 1, broadcast message data is stored in a broadcast data buffer assigned for the subaddress or mode command. Each subaddress or mode command must have an assigned, valid non-zero broadcast buffer address. Non-broadcast message data is stored in Data Buffer A.

There are two ways to deal with broadcast messages in indexed buffer mode:

Option 1 for Index Mode Broadcast Messages:

The first alternative isolates broadcast message information in the broadcast data buffer. If the descriptor Control Word IBR bit and Interrupt Enable Register IBR bit are both set, reception of broadcast messages generates an $\overline{\text{INTMES}}$ interrupt to the host. The broadcast data buffer

must be processed before another broadcast message arrives to prevent loss of data. Broadcast messages do not decrement the INDX register, and Data Pointer A is not updated in message post-processing. This scheme may be well suited for Single Message Mode (INDX = 0) when the host can reliably service either the broadcast data buffer or data buffer A before the next receive message arrives for the same subaddress (or mode code).

Option 1 Setup: At initialization, host asserts NOTICE2 bit in Configuration Register 1 and sets the Control Word IBR (Interrupt Broadcast Received) bit for each index mode descriptor block. The IBR bit is also asserted in the Interrupt Enable Register.

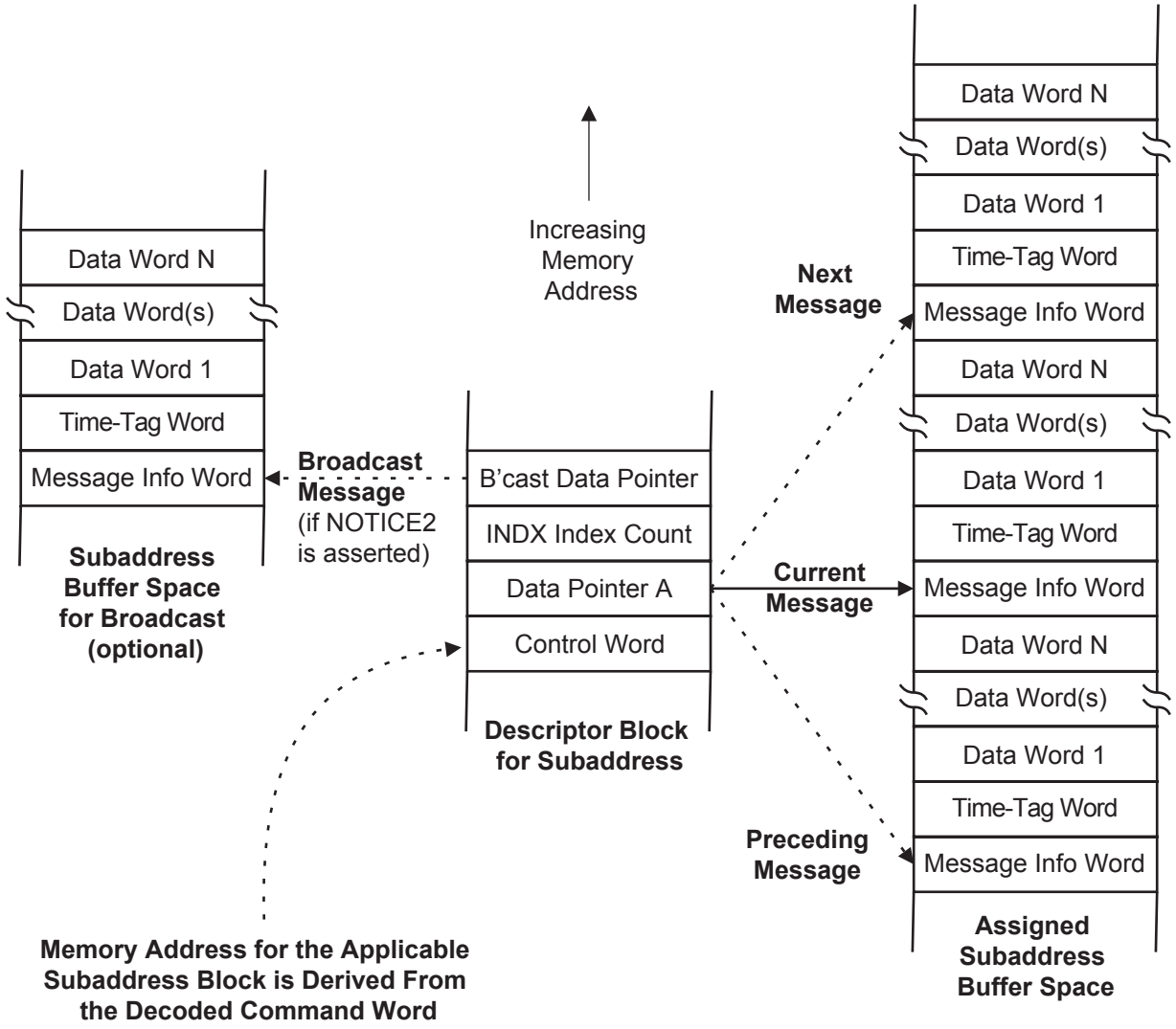
When a broadcast command is received, message information and data are stored in the broadcast data buffer. If descriptor Control Word IBR bit is set, an $\overline{\text{INTMES}}$ interrupt is generated. The host must read the Interrupt Log to determine the originating subaddress (or mode code) then service the broadcast data buffer for that subaddress (or mode code) before the next broadcast message to the same subaddress (or mode code) arrives.

Option 2 for Index Mode Broadcast Messages:

The second alternative stores both broadcast and non-broadcast message information in data buffer A. Optional IBR interrupts can signal arrival of broadcast messages. The RT handles broadcast messages just like non-broadcast messages, except the Message Information Word BCAST bit is asserted to identify broadcast messages during host buffer servicing. All messages decrement the INDX register and Data Pointer A is updated in message post-processing. This scheme is compatible with Single Message Mode or conventional N-message indexing. For Notice II compliance, separation of broadcast and non-broadcast data occurs within the host.

Option 2 Setup: At initialization, host negates the NOTICE2 bit in Configuration Register 1. If broadcast interrupts are used, the Control Word IBR (Interrupt Broadcast Received) bit is asserted at each desired index mode descriptor block. The IBR bit is also asserted in the Interrupt Enable Register.

Using option 2, the host has several options for servicing data buffer A: (a) when INDX decrements from one to zero (using the IXEQZ interrupt), (b) when a broadcast message occurs (using the IBR interrupt) or (c) when any message arrives (using the IWA interrupt).



Upon successful message completion, if non-zero the INDX count in Descriptor Word 3 is decremented. If decremented result is non-zero, Data Pointer A is adjusted so next message is stored above just-completed message. If decremented INDX is zero, Data Pointer A remains static and IXEQZ interrupt occurs if enabled in Control Word.

Figure 12. Illustration of Indexed Buffer Mode

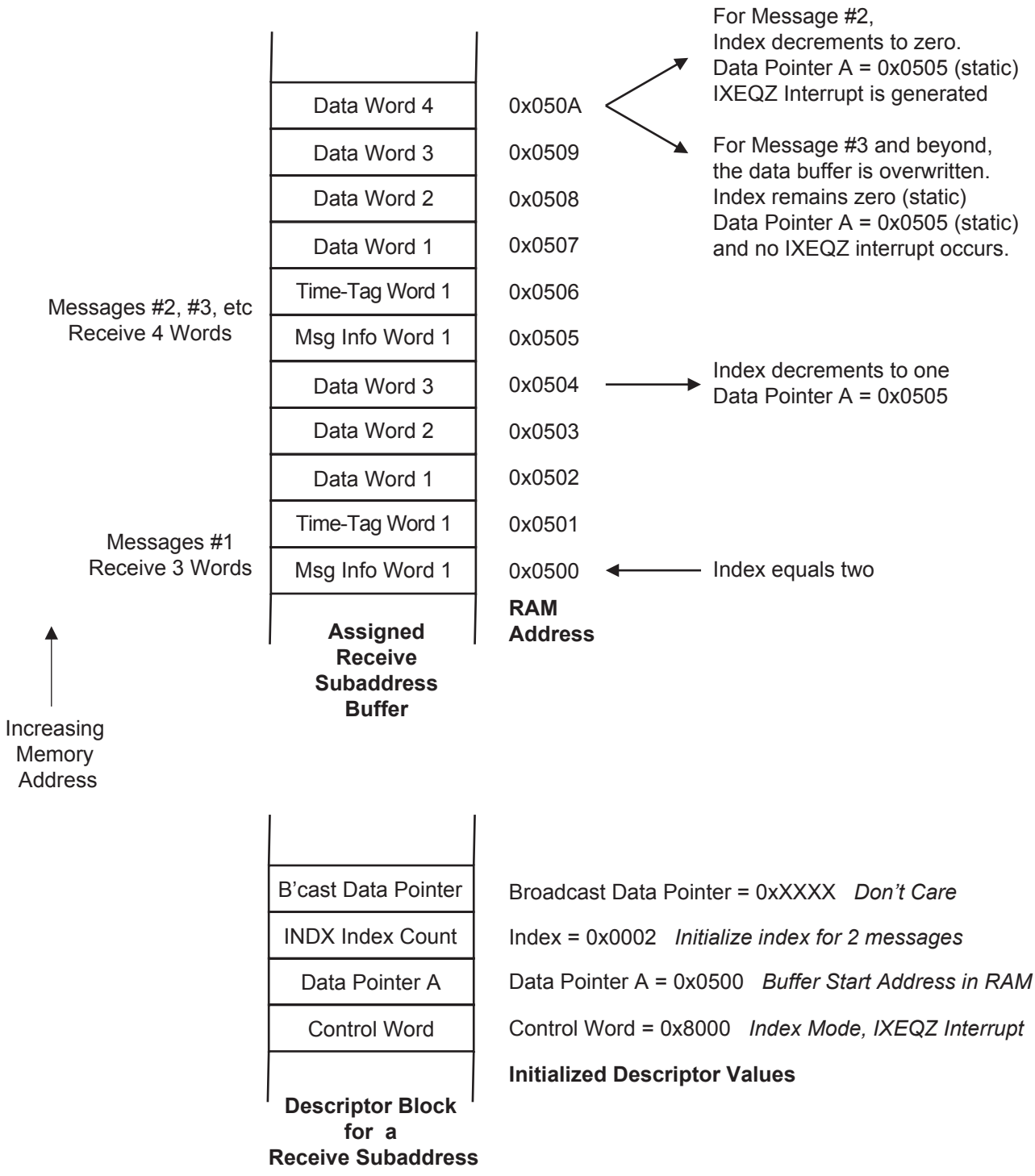


Figure 13. Indexed Buffer Mode Example for a Receive Subaddress (broadcast not enabled)

11.5. Circular Buffer Mode 1

The device offers two circular data buffer modes as alternatives to ping-pong and indexed buffering. These circular buffer options only apply for subaddress commands, not mode code commands. Circular buffering simplifies software servicing of the remote terminal when implementing bulk data transfers. A circular buffer mode can be selected for any subaddress by properly initializing its descriptor Control Word. Circular Buffer Mode 1 is selected when descriptor Control Word PPEN and CIR2EN bits are both 0, and the CIR1EN bit is logic 1.

When a subaddress uses circular buffer mode 1, its four word block in the Descriptor Table is defined as follows:

Descriptor Word 1	Control Word
Descriptor Word 2	SA (Buffer Start Address)
Descriptor Word 3	CA (Buffer Current Address)
Descriptor Word 4	EA (Buffer End Address)

If Descriptor Word 1 is stored at memory address N, Descriptor Word 2 is stored at address N+1, and the other two words are stored at addresses N+2 and N+3.

Figure 14 provides a generalized illustration of Circular Buffer Mode 1, while Figure 15 shows a specific example. Circular Buffer Mode 1 uses a single user-defined buffer that merges all transmit or receive data, along with message information. Two words (Message Information and Time-Tag) are stored at the beginning of the block for each message, followed by the message data word(s). The Mode 1 buffer pointers roll over (are reset to their base addresses) when the allocated data buffer memory is full.

For each valid receive message, the device enters a Message Information word, Time-Tag word and data word(s) into the circular receive buffer. For each valid transmit message, the device enters a Message Information word and a Time-Tag word into reserved memory locations within the circular transmit buffer. The device automatically controls the wrap around of circular buffers.

Two pointers define circular buffer length: start of buffer (lowest address) and end of buffer (highest address). User specifies the start of buffer (SA) by writing the lowest address value into the second word of a unique subaddress descriptor block. The user defines the bottom of the buffer (EA) by writing the highest address value to the fourth word of that unique descriptor block. Both SA and EA remain static during message processing. The third word in the descriptor block identifies the current address CA (i.e., last accessed address plus one). The circular buffer wraps to the start address after completing a message that results in CA being greater than or equal to EA. If CA increments past EA during message processing, the device will access memory addresses greater than the EA value. Reserve 33 address locations past the EA address to accommodate a worst-case 32 data word message with a record starting at address = EA minus 1.

Each receive subaddress and transmit subaddress may have a unique circular buffer assignment. The RT decodes the command word T/$\overline{R}$ bit, subaddress field and word count / mode code field to select the unique command descriptor block containing the Control Word, SA pointer, CA pointer and EA pointer.

For receive messages, the device stores the Message Information word to the address specified by CA, the Time-Tag word into CA+1 and the data into the next “N” locations starting with CA+2. For transmit messages, the device stores the Message Information word to the address specified by CA and the Time-Tag word into CA+1. Retrieval of data for transmission starts at address CA+2. When entering multiple transmit command data packets into the circular buffer, delimit each data packet with two reserved memory locations. The device stores the Message Information word and Time-Tag word into the reserved locations when processing the command.

Message processing for all commands begins with the device reading the unique descriptor block for the subaddress or mode code specified by the T/$\overline{R}$ bit, subaddress and word count fields in the received command word.

For receive messages, the device stores “N” received data words in the circular data buffer. The first data word received is stored at the location specified by the CA pointer +2. After message completion, the device stores the Message Information word and Time-Tag words to addresses CA and CA+1 respectively. If no errors were detected, the device updates descriptor CA register. If the next address location (last stored data word +1) is less than or equal to EA, CA is updated to (last stored address +1). If the next address location (last stored data word +1) is greater than EA, the data buffer is full (or empty); CA is updated to the SA value. If descriptor Control Word IXEQZ bit is asserted (and if Interrupt Enable Register IXEQZ bit is asserted) the device generates an interrupt to indicate full receive buffer by asserting the $\overline{INTMES}$ interrupt output.

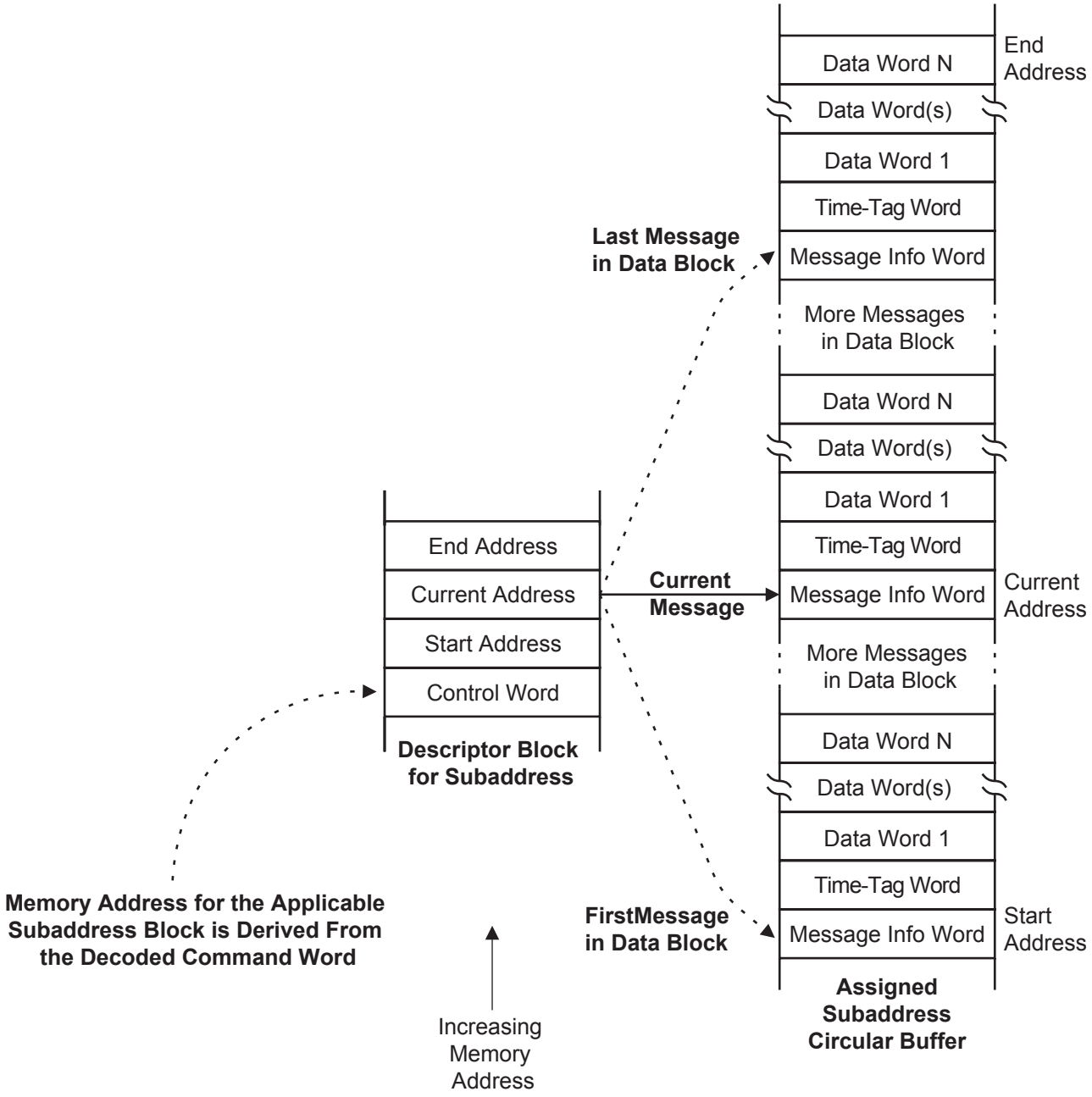
Although all messages store Message Information and Time-Tag words, no data is stored if the message ended with error, or if the Busy status bit was set or if the commend was illegal (example: illegalized word count).

Such messages do not update CA, so the next message overwrites the same buffer space.

For transmit commands, the device begins transmission of data retrieving the first data word stored at address CA+2. (Reminder: addresses CA and CA+1 are reserved for the Message Information and Time-Tag words.) When message processing is complete, the device writes the Message Information and Time-Tag words into the buffer. If no errors were detected, the device updates descriptor CA register. If the next address location (last retrieved data word +1) is less than or equal to EA, CA is updated to (last retrieved address +1). If the next address location (last retrieved data word +1) is greater than EA, the transmit data buffer is empty; CA is updated to the SA value. If the descriptor Control Word IXEQZ bit is asserted (and if the Interrupt Enable Register IXEQZ bit is asserted) the device indicates “transmit buffer empty” by asserting the $\overline{\text{INTMES}}$ interrupt output.

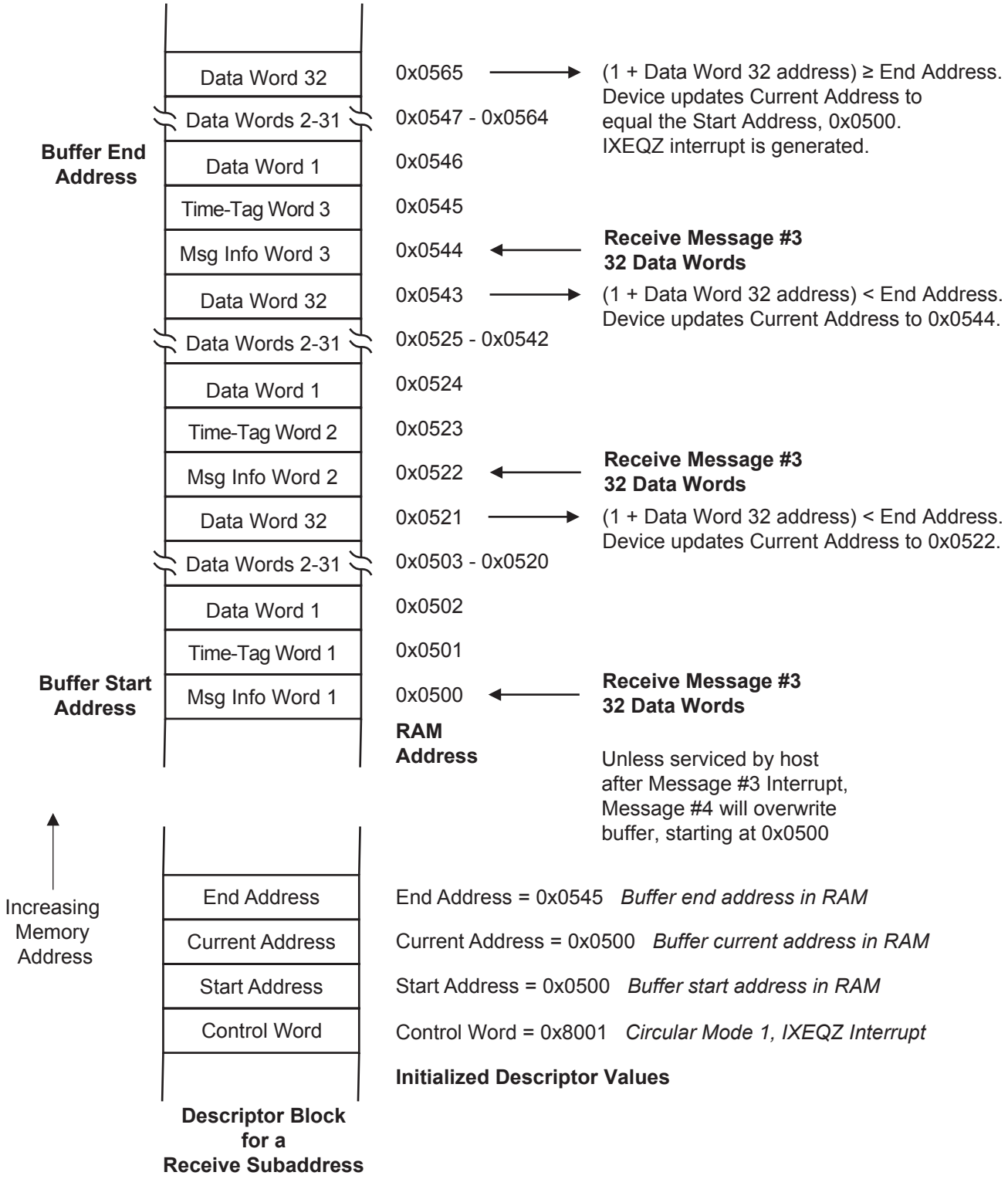
Circular Buffer Mode 1 does not automatically support NOTICE2 segregation of broadcast data, even when the NOTICE2 bit equals 1 in Configuration Register 1. Data from broadcast and non-broadcast receive commands is stored in the same buffer. However Notice 2 for MIL-STD-1553 does not state where data segregation should occur. It is acceptable for the host to separate broadcast and non-broadcast data when offloading the circular buffer. To choose this option, set GPBCST bit 3 in “Configuration Register 2 (0x0001)” on page 24. This enables the BCAST (broadcast) bit 13 in the Message Information Word stored for each message (replacing gap error flag). The BCAST bit in the Message Information Word then reflects broadcast or non-broadcast status for each stored message. If broadcast messages are not expected during data block transmission, the host can illegalize broadcast commands for the subaddress. Broadcast illegalization can be done either permanently, or only when data block transmission is scheduled.

For transmit subaddresses using Circular Buffer Mode 1, occurrences of broadcast-transmit commands to RT31 do not result in bus transmission. However these messages update the Message Information Word addressed by the Current Address (CA) pointer (and following Time-Tag Word) but afterwards, the CA pointer remains unchanged. The next transmit command to the same subaddress, whether broadcast or not, overwrites the Message Information and Time-Tag Word locations written by the previous broadcast transmit command.



Descriptor block is initialized so Current Address equals buffer Start Address. After each successful message transaction, Current Address is adjusted to point past last data word accessed. If adjusted Current Address points past End Address, the Current Address is reinitialized to match Start Address and an optional interrupt is generated to notify host that the pre-determined data block was fully transacted.

Figure 14. Illustration of Circular Buffer Mode 1



Unlike Indexed mode, Data Block completion is based on Buffer Full / Buffer Empty, not number of messages.
Buffer size was purposely sized to yield remaining capacity after 2 full-count messages, to illustrate device behavior.
The circular buffer should have a 33-word pad beyond its End Address to deal with buffer overrun without data loss.

Figure 15. Circular Buffer Mode 1 Example for a Receive Subaddress

11.6. Circular Buffer Mode 2

Circular Buffer Mode 2 segregates message data and message information in separate host-defined buffers. Separating data from message information simplifies the host software that loads or unloads the data to or from the buffer. After a predetermined number of messages has been transacted, buffer address pointers for data and message information are automatically reset to their base addresses. Figure 16 is a generalized illustration of Circular Buffer Mode 2, while Figure 17 shows a specific example.

Circular Buffer Mode 2 is selected when the Control Word PPEN bit is zero and the CIR2EN bit is logic 1. When the CIR2EN bit is high, the CIR1EN bit is don't care. The descriptor Control Word DPB bit is not used.

Any receive subaddress using circular buffer mode 2 has two circular buffers: a data storage buffer and a message information buffer. A separate buffer pair may be used for transmit commands to the same subaddress, if it also uses circular buffer mode 2. Each transmit and receive subaddress using circular buffer mode 2 may have unique data buffer and message info buffer assignments. Careful management (involving the bus controller) may allow buffer sharing, as long as multiple message sequences to a given subaddress are not interrupted by messages to other subaddresses that use the same buffer space.

When a subaddress uses circular buffer mode 2, its Descriptor Table 4-word block is defined as follows:

Descriptor Word 1	Control Word
Descriptor Word 2	SA (Buffer Start Address)
Descriptor Word 3	CA (Buffer Current Address)
Descriptor Word 4	MIBA (Message Info Buffer Addr)

If Descriptor Word 1 is stored at memory address N, Descriptor Word 2 is stored at address N+1, and the other two words are stored at addresses N+2 and N+3. The first word in the descriptor block is the Control Word. The second and third words in the descriptor are the Start Address (SA) and Current Address (CA) pointers. The Message Information Buffer Address (MIBA) points to the storage location for the Message Information Word from the next occurring message.

Each time a message is completed, the device writes a new Message Information Word and Time-Tag Word in the MIB (Message Information Buffer) at the MIBA address and following location, respectively. The MIBA pointer is not updated if message error occurred, if the Busy status bit was set, or if the command was illegalized (for example an illegal word count expressed in the command word.) For these situations, the Message Information and Time-Tag words are still written, but MIB updates for the following message will overwrite the just-written Message Information and Time-Tag word addresses.

For error-free receive messages, received data words are stored in the data buffer after message completion, starting at the CA address value. The CA value is then updated for next-message readiness.

After writing the two MIB words, the device updates the MIBA value to show the buffer address to be used by the next message. Until the predetermined number of error-free messages is transacted, the MIBA value is double-incremented at each update. Before updating the MIBA in Descriptor Word 4, the pre-existing MIBA value is incremented once then checked for 'full count," occurring when all N low-order address bits initialized to zero (explained below) become N "one" bits. Full count means the predetermined number of successful messages was completed. When this occurs, the CA and MIB pointers are automatically written to their initialized values by the device.

To preserve data integrity, the TRXDB bit should be set in Control Register 2 to avoid storing incomplete data from messages resulting in error. With TRXDB asserted, the host is not bothered by message retries caused by errors. The Buffer Empty/Full interrupt (if enabled) is generated only upon successful transaction of the entire N-message data block.

To initialize Circular Buffer Mode 2, the host must know the number of messages to be transacted, always a power of two: 1, 2, 4, 8, 16, 32, 64, 128, 256 or 512 messages. The host writes descriptor Control Word bits 7:4 with an encoded 4-bit value to set the fixed number of messages to be transacted. This is illustrated in Table 9. The host initializes the descriptor block MIBA pointer with a Message Information Buffer starting address. Because the MIB stores two words for each message, the allocated MIB space should equal 2x the number of messages.

The initially-loaded MIB base address value is restricted. Some lower bits of the starting address must be zero so the device can restore the MIBA pointer to the initial MIB base address after the predetermined message count is transacted. As illustrated in Table 9, the required number of logic-0 bits depends on the message count. Initializing the MIBA base address with more trailing zeros than indicated is acceptable; initializing less trailing zeros will cause malfunction.

Allocated space in the data buffer (see column 3, Table 9) assumes each message has the maximum 32 data words. If messages contain less than 32 words, the data buffer size can be reduced. Since Circular Buffer Mode 2 counts messages, values in all remaining Table 9 columns remain valid when message word count is reduced.

The host may read the MIBA value to determine the number of messages that have occurred since initialization. By reading the initially-zeroed lower bits of the MIB Address, the host may determine the number of the next occurring message.

From Table 9, a block of 128 messages requires 8 trailing zeros in the initial MIBA address, for example, 0x0F00. After each message is completed, the MIBA value is updated (0x0F02, 0x0F04, etc.) The device detects message block completion when all required initially-zero trailing address bits equal 1 after MIBA is incremented once. In our example, MIBA would increment from 0x0FFE to 0x0FFF. When “full count” occurs, the device updates MIBA to the original value (e.g., 0x0F00) and copies the SA starting address value to CA current address register, ready for buffer service by the host. The device optionally generates a “buffer empty-full” interrupt for the host when block transfer is completed.

During block transfer, the host can read the MIBA value to determine the number of additional messages needed before the N-message data block is complete.

Message processing for all commands begins with the RT reading the unique descriptor block for the subaddress specified by the T/$\overline{R}$ bit, subaddress and word count fields in the received command word.

Table 9. Circular Buffer Mode 2 (Initialization factors based on message block size)

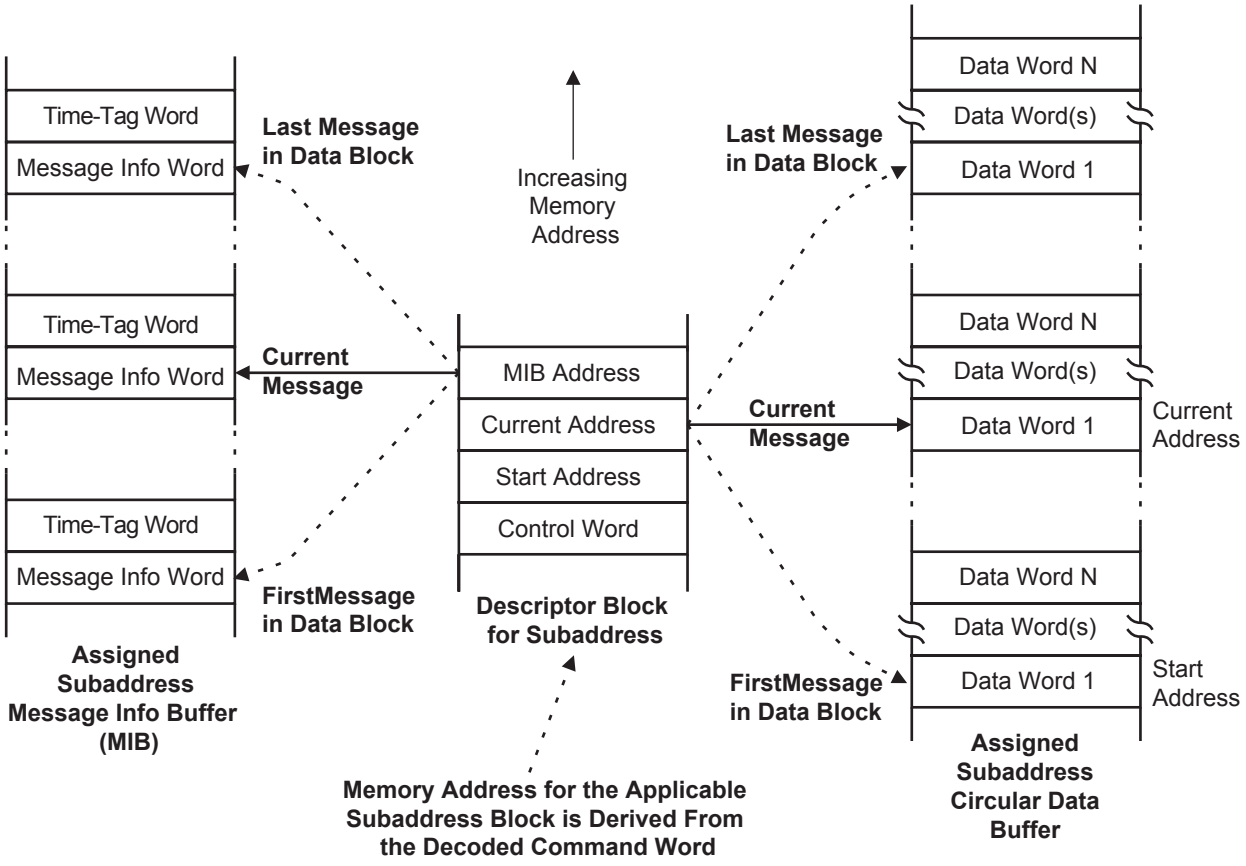
Number of Messages	Control Word Bits 7:4 CIR2ZN Field	Required Data Space if 32 Words / Msg	Required MIB Space, 2 Words / Msg	Initial MIBA Value, Showing the Required Leading and Trailing Zeros
2	0010 (2)	64	4	**0xxxxxxxxxxxx00**
4	0011 (3)	128	8	**0xxxxxxxxxxx000**
8	0100 (4)	256	16	**0xxxxxxxxxx0000**
16	0101 (5)	512	32	**0xxxxxxxxx00000**
32	0110 (6)	1,024	64	**0xxxxxxxx000000**
64	0111 (7)	2,048	128	**0xxxxxxx0000000**
128	1000 (8)	4,096	256	**0xxxxxx00000000**
256	1001 (9)	8,192	512	**0xxxxx000000000**
512	1010 (A)	16,384	1,024	**0xxxx0000000000**

For receive subaddresses using Circular Buffer Mode 2, the device stores received data words in the circular data buffer. The first data word received for each message is stored at the location indicated by the CA pointer. After the correct number of words is received (as specified in the command word) the device writes Message Information and Time-Tag words in the Message Information Buffer then updates the descriptor CA Current Address and MIBA Message Information pointers for next-message readiness. If the predetermined total number of messages has not yet been transacted, MIBA points to the next location in the message information buffer and CA points to the next location in the data buffer. If the completed message is the last message in the block, the CA current (data) address and MIBA message Information pointers are reinitialized to their base address values. (Control Word bits 7:4 tell the device how many MIBA lower bits to reset.) If the descriptor Control Word IXEQZ bit is asserted (and if the Interrupt Enable Register IXEQZ bit is asserted) the device generates a Buffer Full / Empty interrupt, asserting the $\overline{\text{INTMES}}$ interrupt output.

For transmit subaddresses using Circular Buffer Mode 2, the device transmits data from the assigned RAM buffer, starting at the location specified by the CA pointer. The first data word transmitted is stored at the location specified by the CA pointer. After all data words are transmitted (as specified in the command word) the device writes Message Information and Time-Tag words in the Message Information Buffer then updates the descriptor CA Current Address and MIBA Message Information pointers for next-message readiness. If the predetermined total number of messages has not yet been transacted, MIBA points to the next location in the message information buffer and CA points to the next location in the data buffer. If the completed message is the last message in the block, the CA current (data) address and MIBA message Information pointers are reinitialized to their base address values. (Control Word bits 7:4 tell the device how many MIBA lower bits to reset.) If the descriptor Control Word IXEQZ bit is asserted (and if the Interrupt Enable Register IXEQZ bit is asserted) the device generates a Buffer Full / Empty interrupt, asserting the $\overline{\text{INTMES}}$ interrupt output.

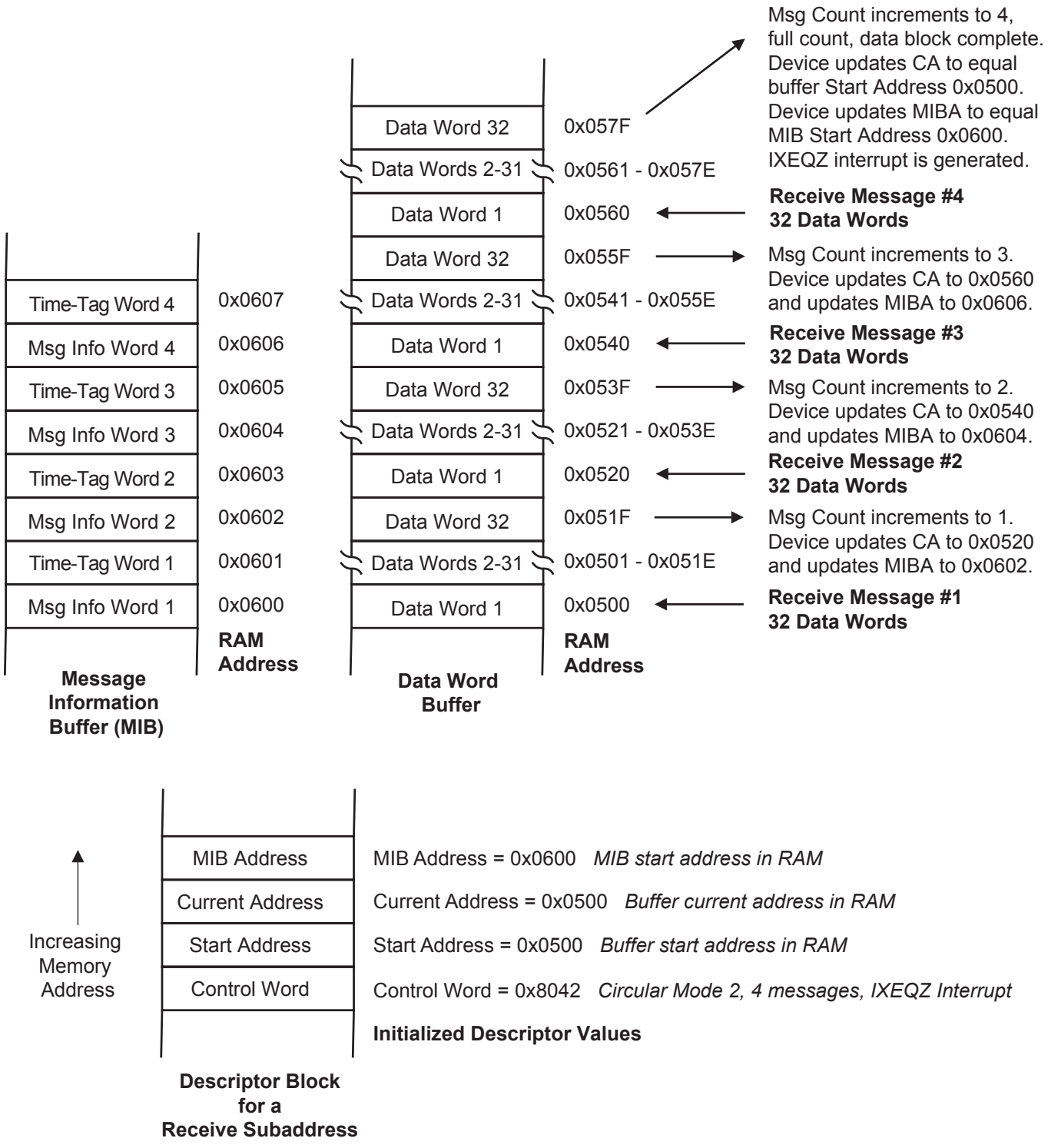
Circular Buffer Mode 2 does not automatically support NOTICE2 segregation of broadcast data, even when the NOTICE2 bit equals 1 in Configuration Register 1. Data words from broadcast receive commands are stored in the same buffer with data from non-broadcast receive commands. However Notice 2 for MIL-STD-1553 does not state where data segregation should occur. It is acceptable for the host to separate broadcast and non-broadcast data when offloading the circular buffer. To choose this option, set GPBCST bit 3 in “Configuration Register 2 (0x0001)” on page 24. This enables the BCAST (broadcast) bit 13 in the Message Information Word stored for each message (replacing gap error flag). The BCAST bit in the Message Information Word then reflects broadcast or non-broadcast status for each stored message. If broadcast messages to the subaddresss are not expected during data block transmission or will result in data block error, the host can illegalize broadcast commands for the subaddress, either permanently or only when block transmission is scheduled.

For transmit subaddresses using Circular Buffer Mode 2, occurrences of broadcast-transmit commands to RT31 do not result in bus transmission. However these messages update the Message Information Word addressed by the Message information Block (MIB) pointer (and the following Time-Tag Word) but afterwards, the MIB and CA pointers remain unchanged. The next transmit command to the same subaddress, whether broadcast or not, overwrites the Message Information and Time-Tag Word locations written by the previous broadcast transmit command.



Segregated storage for data and message information simplifies host loading / offloading of buffered data. Descriptor MIB Address tracks number of messages. Full count occurs when N initialized 0-bits become N 1-bits. When full number of messages in block is transacted, an optional interrupt is generated to notify host.

Figure 16. Illustration of Circular Buffer Mode 2



Data Block completion is based on number of messages, not Buffer Full or Buffer Empty.
Example is set to successfully transact four 32 data word receive messages, then generate IXEQZ interrupt for host.
The data buffer requires minimal processing by host because message information words are stored separately in MIB.

Figure 17. Circular Buffer Mode 2 Example for a Receive Subaddress

12. MODE COMMAND PROCESSING

12.1. General Considerations

The device provides decoding for all mode code combinations, consistent with MIL-STD-1553B requirements. Several mode command options are provided to suit any application requirement:

In Configuration Register 1, the option bit UMCINV (Undefined Mode Codes Invalid) globally defines whether undefined mode code commands are treated as valid (default) or invalid commands. This bit applies only to the following 22 mode code commands that are undefined in MIL-STD-1553B:

Mode Codes 0 through 15 with T/$\overline{R}$ bit = 0
Mode Codes16, 18 and19 withT/$\overline{R}$ bit = 0
Mode Codes 17, 20 and 21 with T/$\overline{R}$ bit = 1

If the UMCINV bit is low (default after $\overline{MR}$ reset) undefined mode code commands are considered valid and RT response is based on individual mode command settings in the Illegalization Table: If the command's table bit equals 0, the mode command is legal; the RT responds "in form" and updates status. If the command's table bit equals 1 the mode command is illegal, the RT asserts Message Error status and (if non-broadcast) transmits only its Status Word without associated data word. Table 10 describes explicit terminal response for each mode code value and command T/$\overline{R}$ bit state, based on various option settings.

If UMCINV is asserted, the 22 undefined mode code commands are treated as invalid: There is no terminal recognition of the command. No command response occurs and status remains unchanged for the benefit of following "transmit status" or "transmit last command" mode commands.

If UMCINV is low, the device determines legal vs. illegal status of commands from the Illegalization Table. If the terminal does not use illegal command detection, the Illegalization Table should be left in its post-reset default state, all values equal logic 0. In this case, the terminal provides "in form" response to all valid commands. The terminal responds with clear status and a transmitted mode data word for mode commands 16-31 with T/$\overline{R}$ bit equals 1. Assigned data buffer locations can be initialized to provide predictable "in form" responses for all transmit mode codes 16-31. (If UMCINV is asserted, the terminal will not respond or update status for received mode codes 17, 20 and 21 with T/$\overline{R}$ = 1.)

To use illegal command detection, the host modifies the Illegalization Table to make illegal any combination subaddress and mode code commands. This may include undefined mode codes, reserved mode codes, and/or mode codes not implemented in the application.

Note: Mode command MC0 "dynamic bus control" cannot be implemented in the device since the HI-6120/21 cannot act as a Bus Controller. Therefore, the "dynamic bus control acceptance" status bit cannot be set in the outgoing status word from this device.

12.2. Mode Command Interrupts

For mode commands, interrupt generation is programmed by the top three bits in the descriptor table Control Word. Notice that broadcast-transmit interrupts can be enabled for mode code values in the range of 0 - 15, but broadcast-transmit mode codes 16 - 31 are not allowed. When a mode command is received and the IWA interrupt bit is asserted in its descriptor Control Word, that command will generate a host interrupt if the IWA bit is high in the Interrupt Enable Register. The IWA bit is asserted in the Pending Interrupt Register and the $\overline{INTMES}$ interrupt output is asserted.

Before $\overline{INTMES}$ interrupt assertion, the device updates the Interrupt Log buffer, writing a new IIW Interrupt Information Word and a new IAW Interrupt Address Word. The IWA (interrupt when accessed) bit is asserted in the new IIW to indicate interrupt type. The IAW contains the Descriptor Table address for the mode command's Control Word, based on mode code value and command word T/$\overline{R}$ bit state. The host reads the IAW to determine the command that caused the interrupt.

12.3. Mode Command Data Words

Mode commands having mode code values from 0 through 15 (decimal) do not have an associated data word. These are received as Command Word only, never having a contiguous data word. The terminal response to valid mode commands 0-15 always consists of Status Word only, assuming command was not broadcast.

Mode commands having mode code values from 16 through 31 (decimal) always have an associated data word. When the command word T/$\overline{R}$ bit equals 0, the terminal receives a data word, contiguously following the Command Word. When valid legal mode commands 16-31 arrive with T/$\overline{R}$ bit equal to 1, the terminal responds by transmitting its status word with a single data word.

When the SMCP option bit in Configuration register 1 is zero, individual data words for mode codes 16-31 decimal are stored in an indexed or ping-pong buffer assigned by the mode command's Descriptor Table entry.

Circular buffer methods are not available for mode code commands.

When the SMCP option bit in Configuration register 1 is asserted, individual data words for mode codes 16-31 decimal are stored within the Descriptor Table itself. This is explained next.

Table 10. Mode Code Command Summary

Command T/$\overline{R}$ bit	Mode Code		MIL-STD-1553 Defined Function	Associated Data Word	Broadcast Allowed	See Note
	Binary	Dec.				
0	00000 to 01111	0 to 15	Undefined mode commands 0 - 15 when T/$\overline{R}$ bit = 0	No	No	(1)
1	00000	0	Dynamic Bus Control	No	No	(3)
1	00001	1	Synchronize (without data)	No	Yes	
1	00010	2	Transmit Status Word	No	No	
1	00011	3	Initiate Self-Test	No	Yes	
1	00100	4	Transmitter Shutdown	No	Yes	
1	00101	5	Override Transmitter Shutdown	No	Yes	
1	00110	6	Inhibit Terminal Flag	No	Yes	
1	00111	7	Override Inhibit Terminal Flag	No	Yes	
1	01000	8	Reset Remote Terminal	No	Yes	
1	01001 to 01111	9 to 15	Reserved Mode Commands 9 - 15 with T/$\overline{R}$ bit = 1	No	Yes	(2)
0	10000	16	Undefined Mode Command	Yes	No	(1)
1	10000	16	Transmit Vector Word	Yes	No	
0	10001	17	Synchronize With Data	Yes	Yes	
1	10001	17	Undefined Mode Command	Yes	No	(1)
0	10010	18	Undefined Mode Command	Yes	No	(1)
1	10010	18	Transmit Last Command	Yes	No	
0	10011	19	Undefined Mode Command	Yes	No	(1)
1	10011	19	Transmit Built-In Test Word	Yes	No	
0	10100	20	Selected Transmitter Shutdown	Yes	Yes	
1	10100	20	Undefined Mode Command	Yes	No	(1)
0	10101	21	Override Selected Transmitter Shutdown	Yes	Yes	

Command T/$\overline{R}$ bit	Mode Code		MIL-STD-1553 Defined Function	Associated Data Word	Broadcast Allowed	See Note
	Binary	Dec.				
1	10101	21	Undefined Mode Command	Yes	No	(1)
0	01001 to 01111	22 to 31	Reserved Mode Commands 22 - 31 with T/$\overline{R}$ bit = 0	Yes	Yes	(2)
1	01001 to 01111	22 to 31	Reserved Mode Commands 22 - 31 with T/$\overline{R}$ bit = 1	Yes	No	(2)

NOTES:

1. The 22 undefined mode commands can be rendered invalid by setting the UMCINV (undefined mode codes invalid) option bit in Configuration Register1. If UMCINV is asserted, there is no recognition of the undefined command by the terminal. If UMCINV is zero, the commands are considered valid. Terminal response when UMCINV equals 0 is wholly determined by the Illegalization Table:
   a. If a command's bit in the Illegalization Table equals zero, the terminal responds "in form" with Clear Status. Mode commands 17, 20 and 21 are undefined when T/$\overline{R}$ bit equals one, but will transmit a contiguous data word. Mode commands 16, 18 or 19 are undefined when T/$\overline{R}$ bit equals 0, but will receive a contiguous data word.
   b. If a command's bit in the Illegalization Table equals one, the command is considered illegal. The Message Error (ME) status bit is asserted and the terminal transmits status without data word. Illegal mode commands 16-31 will not transmit or receive a mode data word.
2. Response to the reserved mode commands is fully defined by Illegalization Table settings. As described in (a) and (b) above, the terminal illegalizes any reserved mode command having Illegalization Table bit equal to 1, and responds "in form" when the Table bit equals zero. The "in form" response for reserved mode commands 16 through 31 transacts a received or transmitted data word.
3. HI-6120/21 cannot fulfill Bus Control duties.

12.4. Standard Mode Command Processing

Data buffer options for mode commands differ from buffer options for subaddress commands. Mode commands can use ping-pong buffering or indexed buffering. When mode commands use indexed buffers, “single message mode” (INDX = 0) is recommended. When using indexed or ping-pong buffers for mode commands:

- For mode commands without associated data word (mode codes 0-15 decimal), only the Message Information and Time-Tag words are updated in the mode command’s assigned data buffer in RAM.
- For mode commands 16-31 (decimal) that receive a data word, indexed and ping-pong buffer methods copy the received mode data word to the mode command’s assigned data buffer in shared RAM, after the message is transacted. The Message Information and Time-Tag words are also updated.
- For most mode commands 16-31 (decimal) that transmit a data word, the device reads the data word for transmit from the buffer location assigned in the Descriptor Table. Exceptions occur for MC18 “transmit last command” and for MC19 “transmit BIT word.” The MC18 data word is automatically provided by the device, based on recent command transactions. The MC19 data word comes from register 0x14 or 0x15, depending on the state of the ALTBITW option in Configuration Register 2. For both MC18 and MC19, the transmitted data word is automatically recorded in the mode command’s assigned data buffer in RAM, after message completion. The Message Information and Time-Tag words are also updated.

12.5. Simplified Mode Command Processing

Mode commands have a data storage alternative that is not available for subaddress commands. The SMCP bit in Configuration Register 1 selects **Simplified Mode Command Processing**, a global option applying to all mode code commands. When the SMCP bit is logic 1, mode command descriptor blocks (in the RT Descriptor Table) do not contain data pointers to reserved buffers elsewhere in RAM. Instead, each 4-word descriptor block itself contains the message information word, the time-tag word and the data from the most recent occurrence of each mode command:

Descriptor Word 1	Mode Command Control Word
Descriptor Word 2	Message Information Word
Descriptor Word 3	Time-Tag Word
Descriptor Word 4	Data Word (mode codes 16-31 only)

Descriptor Word 1 contains the mode code command Control Word. When SMCP is used, just four host-initialized Control Word bits (bits 15-12) are active, These enable message interrupts or force Busy status for the mode command. Just two device-controlled Control Word bits are used: DBAC (descriptor block accessed) and BCAST (broadcast).

When SMCP is enabled, the host only initializes Descriptor Words 1 in the “mode command” latter half of the Descriptor Table, and Descriptor Words 4 for certain transmit mode codes 16-31 decimal, containing transmit mode data word values.

For transmit and receive mode commands without data word (mode codes 0-15 decimal): When SMCP is selected, the host does not initialize Descriptor Words 4. These locations remain at default 0x0000. Further, the host does not initialize device-maintained Descriptor Words 2 or 3. The SMCP logic updates these Message Information and Time-Tag words after message completion, as well as the DBAC (descriptor block accessed) and BCAST (broadcast) bits in Descriptor Word 1.

For transmit mode codes 16-31 (decimal) that transmit a data word: When SMCP is selected, the host does not initialize device-maintained Descriptor Words 2 or 3. The SMCP logic updates these Message Information and Time-Tag words after message completion, as well as the DBAC (descriptor block accessed) and BCAST (broadcast) bits in Descriptor Word 1. The default transmit data value is 0x0000. There are just three defined transmit mode codes in this range: MC16, MC18 and MC19.

- Descriptor Word 4 for mode command MC16 “transmit vector word” should be initialized, if a value other than 0x0000 is needed.
- The MC18 data word is automatically provided, based on the last transacted command. The transmitted data value is copied to the MC18 Descriptor Word 4 after message completion.
- The MC19 data word comes from register 0x14 or 0x15, depending on the state of the ALTBITW option in Configuration Register 2. The transmitted data value is copied to the MC19 Descriptor Word 4 after message completion.

- For the remaining transmit mode codes MC17 and MC20 - MC31, Descriptor Word 4 provides the data word for transmission. Default data value is 0x0000.

For receive mode commands 16-31 (decimal) that receive a data word: When SMCP is selected, the host does not initialize device-maintained Descriptor Words 2 or 3. The SMCP logic updates these Message Information and Time-Tag words after message completion, as well as the DBAC (descriptor block accessed) and BCAST (broadcast) bits in Descriptor Word 1. The SMCP logic copies the received mode data word to Descriptor Word 4 for the specific receive mode command MC16 – MC31.

Section 16 Appendix shows terminal response to all possible subaddress and mode code command combinations. The table summarizes terminal response for the full range of message conditions, including errors, incomplete messages, etc. The table explicitly describes terminal response and impact on terminal Status Word, Descriptor Control Words and data buffer Message Information Words. The table includes effects for all pertinent setup options and identifies all interrupt options available. Bold text blocks indicate error-free messages or “in form” Clear Status responses when the terminal is not using “illegal command detection”.

13. INTERRUPT MANAGEMENT

13.1. Host Message Detection Options

Upon receiving messages, the host has several options.

The individual descriptor table Control Words have enable flags for generating interrupts. Interrupts can be enabled on a subaddress or mode code basis. For any subaddress, interrupts can be enabled for (a) every command occurrence, (b) upon occurrence of broadcast commands, (c) at end of multiple message block transfers (index mode or circular buffer modes only), or (d) no interrupts at all.

Some subaddress commands may not require immediate host servicing. If the number of legal subaddresses is small, the host can poll descriptor table Control Words for the legal subaddresses to detect message activity. The Control Word’s DBAC bit (descriptor block accessed) is set whenever a message is processed. This bit is automatically reset by any host read cycle to the descriptor Control Word. Whenever the DBAC bit reads high, the subaddress transacted a message since the last Control Word read cycle.

Another interrupt alternative that works for any number of legal subaddresses (or when illegal command detection is not used) is to poll the device ACTIVE pin. This pin is high whenever a command is being processed. After the ACTIVE pin goes low, the host can read the Current Command Register to determine the processed command word, or may fetch the command’s descriptor table address from the Current Control Word Address register. Both registers maintain their loaded values until the next valid command to the terminal is decoded.

13.2. Host Interrupt Generation

Interrupts are output signals notifying the host when predetermined events have occurred during terminal operation; the interrupt-causing events are fully programmable. The host defines message-specific interrupt-causing events when initializing the Descriptor Table. Other hardware-based interrupts are configured when internal device registers are initialized.

To manage host interrupts, the device architecture involves an Interrupt Log buffer, three control registers, two interrupt output pins and two interrupt acknowledge input pins. The three internal registers are the Pending Interrupt Register, the Interrupt Enable Register and the Interrupt Log Address Register. The Pending Interrupt Register contains information identifying events programmed by the host to generate interrupts. The Interrupt Enable register lets the host enable or disable interrupt generation for different interrupt-causing events. The Interrupt Log Buffer is a 32-word ring buffer located in shared RAM address range 0x0040 to 0x005F.

Separate interrupt outputs are provided for hardware interrupts ($\overline{\text{INTHW}}$) and message interrupts ($\overline{\text{INTMES}}$). The host programs both pins as either pulsed interrupt outputs or level-sensitive outputs, by writing the INTSEL bit in Configuration Register 1. The states are summarized in Table 11.

Table 11. Summary of Interrupt Outputs.

Config. Register 1 Bit	Interrupt Output Pins	Interrupt Acknowledge Input Pins
INTSEL	$\overline{\text{INTHW}}$ / $\overline{\text{INTMES}}$	ACKHW & ACKMES for HI-6120. ACKINT for HI-6121
0	Pulsed Output Active Low	The ACK pins are not used
1	Level Output Active Low	Active High (Internal pull-downs)

Pulsed outputs have brief (~250ns) duration, sufficient to drive edge-triggered host inputs. In the level mode of operation, asserted interrupts remain low until acknowledged by the host. For HI-6120 the host acknowledges level interrupts by asserting the ACKHW or ACKMES input pin to clear the respective interrupt $\overline{\text{INTHW}}$ or $\overline{\text{INTMES}}$ output. For HI-6121, assert the ACKINT pin to clear both $\overline{\text{INTHW}}$ and $\overline{\text{INTMES}}$ output pins to the high state.

Assertion of the $\overline{\text{INTHW}}$ interrupt indicates an interrupt-causing hardware event that is enabled in the Interrupt Enable Register. Defined interrupt-causing events are listed in Table 12. When the $\overline{\text{INTHW}}$ output is asserted, one or more bits are set in the Pending Interrupt Register, to identify the interrrupt event(s).

Assertion of the $\overline{\text{INTMES}}$ interrupt after a message is completed indicates a predetermined message event occurred that is (1) globally enabled in the Interrupt Enable Register and (2) specifically enabled for the last command transacted. The Descriptor Table Control Word for each command is programmed by the host to enable events that generate message interrupts. The type of $\overline{\text{INTMES}}$ event is reflected in the IXEQZ, IWA, IBR, ILCMD and MERR bits within the Pending Interrupt Register.

The interrupt architecture maintains information for the last 16 interrupts in a 32-word ring buffer. The device automatically handles interrupt-logging overhead. Each interrupt generates two words of information to help the host perform interrupt processing. The Interrupt Identification Word (IIW) identifies the type(s) of interrupt that occurred. The Interrupt Address Word (IAW) identifies the interrupt source (e.g., subaddress Descriptor Block) using a 16-bit address.

13.2.1. Interrupt Log Address Register

Bits 7:0 in this register indicate the IIW storage address within the buffer for the next occurring interrupt, 0x0040 to 0x005E. Bits 15:8 indicate the number of interrupts since the register was last read. For further details, see the full description of the Interrupt Log Address Register.

13.2.2. Interrupt Address Word (IAW)

Stored in the Interrupt Log Buffer, Interrupt Address Words (IAW) identify interrupt-causing messages by storing the descriptor block address for the subaddress or mode code command that generated each message interrupt.

13.2.3. Interrupt Identification Word (IIW)

Stored in the Interrupt Log Buffer, Interrupt Identification Words identify type of interrupt event. Bit assignments match those used in the Pending Interrupt Register. The host or subsystem reads the IIW to determine which type of interrupt occurred. The Interrupt Identification Word is defined in Table 12.

Table 12. Interrupt Identification Word

IIW - Interrupt Identification Word			IAW - Interrupt Address Word
Bit	Interrupt	Origin	
15	IXEQZ	Message	IAW contains the Command Word Descriptor Table Address
14	IWA	Message	
13	IBR	Message	
12	--------	--------	
11	--------	--------	
10	MERR	Message	
9	--------	--------	
8	ILCMD	Message	
7	SPIFAIL	Hardware	IAW contains 0x0000
6	LBFA	Hardware	
5	LBFB	Hardware	
4	TTINT1	Hardware	
3	TTINT0	Hardware	
2	RTAPF	Hardware	
1	EECKF	Hardware	
0	RAMIF	Hardware	

14. RESET AND INITIALIZATION

This section describes the hardware and software reset mechanisms. Hardware Master Reset returns the device to the uninitialized state, requiring register/RAM initialization before terminal execution can begin. Initialization can be performed by the host after $\overline{MR}$ reset, or automatically, at the user's option, by reading configuration data from an external serial EEPROM. Software reset is asserted by setting the SRST bit in Configuration Register 1. Software reset has minimal effect on previously initialized registers and RAM structures that define terminal behavior. However some reinitialization may be needed for some applications, after SRST reset is complete.

14.1. Master Reset using the $\overline{MR}$ pin and Optional Auto-Initialization

Hardware master reset is initiated by a low to high transition on the $\overline{MR}$ pin; it should be applied after power-up, but may be used anytime afterward. When asserted, the $\overline{MR}$ input pin causes immediate, unconditional hardware reset. Command processing is terminated, the bus decoders and encoder are cleared, the Time-Tag count is reset. The Message Error, Busy and Broadcast Command Received status bits are reset and Terminal Flag bit is enabled for assertion. All internal logic is cleared. Registers and RAM structures are restored to the states shown in Table 13. The READY, ACTIVE, $\overline{INTMES}$ and $\overline{INTHW}$ output pins are negated if previously asserted.

After $\overline{MR}$ pin low to high transition, these steps occur:

1. After 200ns, the states of the following input pins are latched into the Operational Status register: RTA4-RTA0, RTAP, AUTOEN, LOCK and INTSEL. Before READY assertion, a host read cycle to any address returns the value in the Operational Status register.
2. If the MTSTOFF pin is logic zero, the device performs a memory test (< 985us). If memory error occurs, the BMTF bit is set in the BIT Word Register 0x0014. If the MTSTOFF pin is logic one, the memory test is bypassed. This option might be chosen if a faster reset process is needed. Regardless of MTSTOFF state, all RAM locations above address 0x001F are cleared to 0x0000.
3. After internal processes are initialized, the device checks the latched state of the AUTOEN bit in the Operational Status register:

If the Operational Status register AUTOEN bit reads low, auto-initialization is bypassed. The host must initialize the terminal as follows:

a. The device asserts the READY output pin. This state change indicates the host can begin post-$\overline{MR}$ reset initialization of registers and RAM structures.

b. Upon READY assertion, the host should initialize configuration and option registers, the Descriptor Table(s) and the Illegalization Table. Initialization may include data written into the various transmit subaddress buffers assigned by the initialized Descriptor Table.

c. After the host completes initialization, it must assert the STEX (start execution) bit in Configuration Register 1 to begin Remote Terminal operation.

If the Operational Status register AUTOEN bit reads high, the device initializes itself from an external serial EEPROM via the dedicated EEPROM SPI port:

The READY output pin remains low while automatic self-initialization proceeds. The device reads initialization data from the external serial EEPROM memory, using the dedicated EEPROM SPI port. Initialization includes all registers, all tables (including secondary Descriptor Tables, if used) and can include initial data written to transmit subaddress data buffers allocated by the Descriptor Table.

If the EE1K pin is low, initialization covers the full 32K address range 0x0 to 0x7FFF, including the entire RAM. Therefore it can initialize secondary Descriptor Tables and transmit subaddress buffers in the upper RAM space. (Note: Typical auto-initialization time is 63ms).

If the EE1K pin is high, initialization covers just the 1K address range 0x0 to 0x003F. This covers all registers and the minimum set of required tables, including the default Descriptor Table from 0x00200 to 0x003FF. For many applications, this is the only Descriptor Table. (Note: Typical auto-initialization time is 1.97ms).

During auto-initialization, the written value for each register or RAM location is read back for confirmation. If the read-back value does not match the corresponding value from EEPROM, an initialization error is saved. This error results in action (described below) that occurs when the initialization process is finished.

While performing initialization, a running checksum is tallied as follows, using EEPROM data read from the 1K or 32K address range. A properly configured serial EEPROM contains a 16-bit checksum value stored at the pair of EEPROM locations correspond-

ing to RAM address 0x0020. The stored checksum is tallied as if RAM address 0x0020 equals 0x0000 and five registers are excluded from checksum computation: Operational Status register 0x0002, Pending Interrupt register 0x0006, Time-Tag register 0x0008 and BIT Word register 0x0014. The stored value is actually the twos-complement of the 16-bit memory checksum, ($\overline{\text{CHECKSUM}}$ + 1).

During initialization, byte pairs are sequentially read from EEPROM, then merged to a 16-bit value that is both written to device RAM (or register) and added (running tally) to the twos-complemented checksum value. When the full 1K or 32K EEPROM range is tallied, the running checksum tally should equal zero, indicating error-free checksum tally. After initialization (at READY assertion), the 16-bit twos-complement checksum value is copied from EEPROM to device RAM address 0x0020. This is part of the Temporary Receive Data Buffer, which does not interfere with terminal initialization.

When the device completes auto-initialization, the READY output pin is asserted to the high state.

If an initialization error occurred, the following events take place immediately after READY assertion:

1. The $\overline{\text{INTHW}}$ interrupt output pin is asserted.
2. The Operational Status Register 0x0002 is written to indicate the type of error. The EECKF or RAMIF bit is set to show checksum failure or read-back data mismatch between RAM and EEPROM.
3. The EELF bit is set in the Built-In Test Word Register 0x0014.
4. If RAMIF read-back error occurred, the address of the first occurring instance is written to register address 0x001F. Additional locations beyond the saved address may have mismatch, but only the first instance is logged.

The STEX bit in Configuration Register 1 is still zero.

If the STEX bit in the initialization EEPROM is high, and if the EECKF, RAMIF and RTAPF bits are reset in the Operational Status Register 0x0002, the device now sets the STEX bit to start Remote Terminal operation. This means: (1) auto-initialization was error-free and (2) the RT address in Operational Status Register bits 15-10 has correct parity. The register's terminal address bits reflect input pin states if the LOCK pin is high, or were overwritten by values from the initialization EEPROM, if the LOCK pin is low.

If automatic STEX assertion was blocked because EECKF or RAMIF bits were written high after READY assertion, the host can write STEX high, overriding the error condition. If STEX assertion was blocked because of RT address parity error, the STEX bit cannot be asserted until the parity error is corrected. The host may overwrite the Operational Status Register RTAP4-0 and RTAP bits to correct the error, then assert the STEX bit in Configuration Register 1.

If the STEX bit in the initialization EEPROM is low, the STEX bit in Configuration Register 1 is not asserted at this time. The device awaits STEX assertion by a host write to Configuration Register 1 before starting Remote Terminal operation. The STEX bit may be written any time after the READY output pin goes high.

After any $\overline{\text{MR}}$ master reset, the state of certain input pins (AUTOEN, LOCK and terminal address pins RTA4 to RTA0 and RTAP) are latched into Operational Status Register 0x0002. Because auto-initialization follows master reset, the mirrored pin states may be overwritten by the values stored in the initialization EEPROM bytes corresponding to register address 0x0002, only if the LOCK input pin is low.

A method for programming the EEPROM itself from a fully configured terminal is explained in a following section entitled "Serial EEPROM Programming Utility". If a different method is used for writing the serial EEPROM, the twos-complemented checksum (described earlier) must be saved in EEPROM locations corresponding to device RAM address 0x0020.

A compatible serial EEPROM uses a SPI interface for byte-access read and write operations. Sixteen-bit register and RAM values in the HI-612X are stored as upper and lower bytes in the EEPROM, in "big endian" fashion. For example, the upper byte for register address 0x0000 is stored at EEPROM address 0x0000 while the lower byte is stored at EEPROM address 0x0001. A 64K x 8 EEPROM is required to store the entire 32K x 16 address range.

Serial EEPROM data mapping follows the device memory map shown in Figure 2. The single exception: two EEPROM locations corresponding to device RAM address 0x0020 must contain the expected checksum value. The serial EEPROM used for auto-initialization should be fully written to cover the HI-6120/21 upper address limit of 0x7FFF (or 0x03FF, depending on the state of the EE1K input pin). Ideally the EEPROM image will reflect a post-$\overline{\text{MR}}$ reset followed by fresh initialization with nothing written to reset-cleared registers or RAM as a result of command processing.

Table 13. Summary of Changes Due to $\overline{MR}$ Master Reset or SRST Software Reset

Hex Address	Device Register	Contents after $\overline{MR}$ Reset	Contents after SRST Reset
0x0000	Configuration Register 1	0x0000	no change
0x0001	Configuration Register 2	0x0000	no change
0x0002	Operational Status Register	bits 7:0 reset to 0x00 bits 15:8 match pins	no change
0x0003	Current Command Register	0x0000	no change
0x0004	Current Control Word Address Register	0x0000	no change
0x0005	Descriptor Table Base Address Register	0x0200	0x0200
0x0006	Pending Interrupt Register	0x0000	no change
0x0007	1553 Status Word Bits Register	0x0000	0x0000
0x0008	Time-Tag Register	0x0000	0x0000
0x0009	Interrupt Log Address Register	0x0040	no change
0x000A	Current Message Information Word Register	0x0000	no change
0x000B-0x000E	Reserved	0x0000	no change
0x000F	Memory Address Pointer (HI-6121 Only)	0x0000	no change
0x0010	Interrupt Enable Register	0x0007	no change
0x0011	Time-Tag Utility Register	0x0000	no change
0x0012	Bus A Select Register	0x0000	no change
0x0013	Bus B Select Register	0x0000	no change
0x0014	Built-In Test (BIT) Word Register	**See Note 1**	0x0000
0x0015	Alternate BIT Word Register	0x0000	no change
0x0016	Test Control Register	0x0000	0x0000
0x0017	BIST Control Register	0x0000	0x0000
0x0018	Loopback Test Transmit Data Register	0x0000	0x0000
0x0019	Loopback Test Receive Data Register	0x0000	0x0000
0x0020-0x001F	Reserved	0x0000	no change

Hex Address	RAM Structure	Contents after $\overline{MR}$ Reset	Contents after SRST Reset
0x0020-0x003F	Temporary Receive Data Buffer, 32 Words	all 0x0000	no change
0x0040-0x005F	Interrupt Log Buffer, 32 Words	all 0x0000	no change
0x0060-0x00FF	Unallocated RAM, 160 Words	all 0x0000	no change
0x0100-0x01FF	Illegalization Table, 256 Words	all 0x0000	no change
0x0200-0x03FF	Descriptor Table (Primary), 512 Words	all 0x0000	**See Note 2**
0x0400-0x7FFF	Host-Assigned Data Buffers	all 0x0000	no change
	Secondary Descriptor Tables, if used	all 0x0000	no change

Terminal Function	Contents after $\overline{MR}$ Reset	Contents after SRST Reset
Hardware Bus Decoders	reset	reset
Hardware Encoders and Transmitters	reset	reset
Command Processing & ACTIVE Output	reset	reset
Terminal Status (incl ME & BCR bits)	reset	reset
Prior Bus Shutdown by Mode Cmd MC4 or MC20	overridden	overridden
Prior Terminal Flag Inhibit by Mode Cmd MC6	overridden	overridden
READY Output	reset	set
$\overline{INTMES}$ & $\overline{INTHW}$ Interrupt Outputs	negated (high)	negated (high)

NOTES:

1. After Master Reset, bits 15, 14 and 2 in the BIT Word Register depend on input pin settings. See register description. If the MTSTOFF input pin is low, register bit 3 (BMTF) depends on memory test outcome. The remaining bits are unconditionally reset. However if auto-initialization is enabled and EEPROM load failure occurs during the subsequent initialization process, register bit 1 (EELF) will be set.
2. Upon SRST reset, the DBAC, DPB, MKBUSY and BCAST bits are reset for each of the 128 Control Words in the primary Descriptor Table which starts at address 0x0200. If secondary Descriptor Tables are used (above address 0x0400), the host must perform any necessary table reconfiguration after SRST reset.

14.2. Software Reset

Software reset is initiated by a host write that sets the SRST bit in Configuration Register 1. This bit is set automatically when a “Reset Remote Terminal” mode command is received while the MCOPT0 bit is set in Configuration Register 2 (0x0002). Software reset causes immediate reset without overwriting registers or tables that were initialized by the host to define terminal behavior. Changes to registers and RAM are summarized in Table 13. Software reset cannot initiate automatic self-initialization from serial EEPROM. Once the SRST bit in Configuration Register 1 is asserted, the following steps are performed:

1. The READY, ACTIVE, $\overline{\text{INTMES}}$ and $\overline{\text{INTHW}}$ output pins are negated. Terminal execution stops while SRST reset is underway. Command processing is terminated. The hardware bus decoders and hardware encoder are cleared. The Message Error and Broadcast Command Received flags in the internal status register used for MC2 or MC18 mode command responses are not affected by SRST.
2. The Descriptor Base Address register (0x0005) is reinitialized to the base address 0x0200. The following registers are cleared: the 1553 Status Word Bits register (0x0007), the Time-Tag register (0x0008) and test registers 0x0016 to 0x0019.
3. The BIT Word Register (0x0014) is cleared, except the contained RTAPF bit is not changed. This reinstates any bus previously shutdown by mode code commands MC4 or MC20 (decimal). If the Terminal Flag status bit was previously inhibited by mode command MC6, inhibit is cleared: The Terminal Flag status bit will be transmitted whenever bit 0 is set in the 1553 Status Word Bits Register.
4. All 128 descriptor table Control Words are modified to reset the DBAC, DPB, MKBUSY and BCAST bits. Subaddresses or mode codes using ping-pong or single message index mode (INDX = 0) are ready for immediate operation after SRST reset is complete. However the device cannot reinitialize the Descriptor Table to restore multi-message block transfers, for indexed buffer mode when initial INDX value was non-zero, or for either circular buffer mode.
5. The device asserts the READY output pin. Terminal operation automatically resumes if the STEX bit in Configuration Register 1 was set before SRST occurred.
6. After READY assertion, the host may reset STEX, then reinitialize all or part of the Descriptor Table. The host can reinitialize the Descriptor Table for subaddresses using multi-message block transfers (Circular Buffer Mode 1, Circular Buffer Mode 2 or Indexed Buffer Mode with initial non-zero INDX.) The host can also reinitialize transmit data in the assigned transmit subaddress data buffers. Data buffers in RAM contain data values loaded before SRST occurred. The host can clear or overwrite this old data. The host can then assert the STEX bit in Configuration Register 1 to restart terminal operation.

14.3. Reset Remote Terminal Mode Code

Mode code MC8 with T/$\overline{\text{R}}$ bit = 1 should reset the Remote Terminal. After Status Word transmission, the device automatically resets the status Message Error (ME) and Broadcast Command received (BCR) bits in its internal status register. Bits 0, 14 and 15 are reset in the BIT Word register at address 0x0014. If either transmitter was shutdown by a previous mode code MC4 or MC20, the shutdown condition is overridden. If the Terminal Flag (TF) status bit was inhibited, the inhibit is reset. This command does not reset any of the host-programmed registers that configure the terminal for operation.

To complete the reset process, the host must assert either $\overline{\text{MR}}$ master reset (with or without auto-initialization) or assert the SRST bit in Configuration Register 1 to execute software reset. Since MC8 requires host interaction, most applications will probably utilize the IWA interrupt to alert the host when valid MC8 is received.

Per MIL-STD-1553B appendix 30.4.3, any reset initiated by the “Reset Remote Terminal” mode command should be completed within 5 ms following transmission of the Status Word. Overall reset time includes internal device initialization, either host initialization or auto-initialization. Overall time to complete reset initiated by the “Reset Remote Terminal” mode command MC8 is affected by host response speed and application complexity.

14.4. Serial EEPROM Programming Utility

The HI-6120 or HI-6121 can program a serial EEPROM via the dedicated EEPROM SPI port for subsequent auto-initialization events. The device copies host-configured registers and RAM (configuration tables and possibly data buffers) to serial EEPROM.

Compatible SPI serial EEPROMs are 3.3V, operate in SPI modes 0 or 3 and and have 128-byte pages. The serial SPI data is clocked at 8.3 MHz SCK frequency. A 2K x 8 EEPROM can restore the lower 1K x 16 device address space. A 64K x 8 EEPROM can restore the entire 32K x 16 device address space.

A deliberate series of events initiates copy of data from HI-6120 or HI-6121 to serial EEPROM. This reduces the likelihood of accidental EEPROM overwrites. **Note: The RT address must have correct (odd) parity before EEPROM read or write can occur.** This series of events must occur to initiate programming:

1. **If using a fresh host initialization immediately following $\overline{MR}$ master reset as the basis for EEPROM copy:** With the AUTOEN, TXINHA and TXINHB pins in logic zero state, apply MR master reset and wait for READY output assertion. Verify that the INTHW output does not pulse low at READY assertion, indicating likely RT address parity error at the RTA4:0 and RTAP pins. Using known good parameters, the host initializes device registers, the RAM descriptor table and transmit data buffers (if necessary). Do not assert STEX. Go to step 3.

   OR

2. **If using the existing EEPROM configuration as the baseline for a new EEPROM configuration:** With the AUTOEN pin in logic 1 state and the TXINHA and TXINHB pins in logic zero state, apply MR master reset and wait for READY output assertion. Verify that the INTHW output does not pulse low (or go and remain low) at READY assertion. Confirm that the RTAPF, EECKF and RAMIF bits are all logic 0 in the Operational Status Register 0x0002. If the STEX bit in Configuration Register 1 was set by auto-initialization, reset it now. Modify register and RAM values to reflect the new changes. Go to Step 3.

3. IMPORTANT: Any processing of valid bus commands between $\overline{MR}$ master reset and this point will cause auto-initialization checksum failure later, due to non-zero values written to read-only registers as a result of command processing. The device will not enter EEPROM copy mode at step 4 if valid command reception caused ACTIVE output assertion after MR reset occurred. If set, the STEX bit in Configuration Register 1 also locks-out EEPROM copy mode at programming step 4.

4. The host writes one of two 2-part “unlock codes” to RAM address 0x0020. The two unlock codes perform identical EEPROM programming with the exception of the programmed state for the STEX bit in Configuration Register 1.

   If auto-initialize should program Configuration Register 1 STEX bit to logic 0, RAM address 0x0020 is first written 0xA5F0, then a second load to 0x0020 overwrites the value just written with 0x5F0A.

   If auto-initialize should program Configuration Register 1 STEX bit to logic 1, RAM address 0x0020 is first written 0x5A0F, then a second load to 0x0020 overwrites the value just written with 0xA0F5.

   In either case, the two unlock writes must occur without intervening access to other device addresses, except Memory Address Pointer 0x000F for HI-6121.

5. The EECOPY input pin is driven high for at least 1 ms, then driven low. In response, the READY output goes low while EEPROM memory is written. Programming commences. The unlock code at address 0x0020 is cleared, then device register and RAM contents are written to the serial EEPROM. During programming, the twos-complemented checksum is tallied for the entire address range being programmed (1K or 32K words), excluding addresses 0x0002, 0x0006, 0x0008, 0x0014 and 0x0020. At EEPROM programming completion, the final checksum is stored in the pair of EEPROM locations corresponding to device RAM address 0x0020. The value written to EEPROM is actually the twos-complement of the memory checksum, (CHECKSUM + 1). The value in EEPROM is used for error detection when performing auto-initialization. (The host can only access the stored value immediately after an auto-initialization sequence is performed. The twos-complement EEPROM checksum value will be copied into RAM address 0x0020.)

6. When the READY output goes high, EEPROM copy is complete. The STEX bit is reset in device Configuration Register 1.

7. The address range copied during EEPROM programming depends on the state of the EE1K input pin when rising edge occurs on the EECOPY input:

   If EE1K is high when EECOPY is asserted, the lower 1K x 16 address range from 0x0 to 0x03FF is copied from device registers and RAM to EEPROM. This includes all registers, all configuration tables in RAM and the primary Descriptor Table in RAM at address 0x0200 to 0x03FF. The 1K x 16 write to EEPROM requires up to 83 ms.

   If EE1K is low when EECOPY is asserted, the entire 32K x 16 address range from 0x0 to 0x7FFF is copied from device registers and RAM to EEPROM. This range covers all registers, all configuration tables in RAM, the primary Descriptor Table in RAM at address 0x0200 to 0x03FF. As long as EE1K remains low when auto-initialization occurs, the 32K x 16 programming option can initialize secondary Descriptor Tables above address 0x0400, if used.

The 32K x 16 write to EEPROM requires up to 2.64 seconds.

The 32K x 16 programming option (EE1K equals zero) can also initialize fixed data for any subset of the 32 possible transmit subaddress buffers, using any of the defined data buffer schemes. To enable EEPROM copy for transmit subaddress data buffers, the buffer space must be pre-loaded with the desired data. Be sure to reserve space for Message Information and Time-Tag Word locations, as required for the transmit subaddress buffer method.

14.5. MIL-STD-1760: Busy Status Assertion After Power-Up

A MIL-STD-1760 Remote Terminal must be able to respond on the bus within 150ms following power turn-on. Acceptable responses are described below. At 500ms following power turn-on, the MIL-STD-1760 RT must respond with data as defined by the MIL-STD-1760 standard, with “Busy” status bit reset. The RT host processor must be fully operational at this time.

Between 150 and 500ms following power turn-on, there are two acceptable ways for the MIL-STD-1760 Remote Terminal to respond to valid messages:

- The RT may respond Clear Status with valid data.
- The RT may respond with the “Busy” bit set in the RT Status Word. This indicates the RT is awake but not ready to transfer data. When Busy status is set, no data is transacted. For receive commands (RT receiving data) any data accompanying the Command Word should be ignored. For transmit commands (RT transmits data), transmission of data is suppressed when Busy status applies; only the busy Status Word is sent in response to valid commands. The HI-612x automatically suppresses RT data transmit when Busy status applies.

In most cases, the second form of RT response is required. The HI-612x can be set up for Busy status two ways: (1) global Busy response to all valid commands, or (2) Busy response to valid commands for selected subaddresses, with Busy status cleared when responding to commands for other subaddresses.

To globally respond Busy status for all valid commands, the host sets Busy status bit 3 in the “1553 Status Word Bits Register (0x0007)”. This single register bit enables/disables the transmitted Status Word flag and suppresses data word transmission for RT transmit commands.

To enable Busy response only for selected transmit or receive subaddresses, the host sets the MKBUSY bit 12 in “Transmit Subaddress Control Word” or “Receive Subaddress Control Word” found in the RT Descriptor Table. The MKBUSY bit must be set in each Control Word individually. This setup may be acceptable when the range of legal transmit or receive subaddresses is limited.

Global Busy status response for all valid commands is the easiest to apply. After power-on reset, the host can initialize the HI-612x by writing register and RAM under program control. Early in that sequence, the host would set Busy status bit 3 in the “1553 Status Word Bits Register (0x0007)”, then assert the STEX “start execution” bit 8 in “Configuration Register 1 (0x0000)” to enable RT responses. To comply with MIL-STD-1760, execution should be enabled within 150ms following power-on. When the RT is fully configured for normal operation, the host should reset the Busy bit in the “1553 Status Word Bits Register (0x0007)”.

Or, if the AUTOEN pin is high, the device performs auto-initialization from pre-programmed serial EEPROM. Of course the EEPROM can be written to configure the RT for global Busy status (or subaddress-specific Busy status) with RT “start execution” enabled. When the AUTOEN pin is high, auto-initialization from EEPROM occurs after completion of a RAM memory test. Initialization data is read from the previously-written external EEPROM and copied into the entire register and RAM address range, 0x0000 to 0x7FFF. Starting at reset rising edge, RAM memory test requires 1.5ms; the following auto-initialization needs 63.1ms, well within the 150ms window for RT response required.

Before 500ms following power turn-on, the MIL-STD-1760 RT must be ready to respond with data as defined by the MIL-STD-1760 standard, with “Busy” status bit reset. The RT host processor must be fully operational at this time. After completing system initialization, the host should deactivate global Busy status by clearing Busy bit 3 in the “1553 Status Word Bits Register (0x0007)”. If individual subaddresses were busied-out, the MKBUSY bit is reset in affected subaddress Control Words in the Descriptor Table.

15. HOST INTERFACE

15.1. HI-6120 Host Bus Interface

The HI-6120 uses a parallel bus interface for communications with the host. Host interface to registers and RAM is enabled through the Chip Enable ($\overline{CE}$) pin, and accessed via 16-bit data bus and several host-originated control signals described below. Timing is identical for register operations and RAM operations via the host bus interface, but read and write operations have different signal timing. The HI-6120 parallel host bus interface is capable of faster communication than the HI-6121 Serial Peripheral Interface.

Depending on the chosen microprocessor family, the processor's hardware bus interface may be described as an "external bus interface," "memory interface" or may have a different name. The user can also implement a software controlled "bit-banged" interface to the HI-6120, at the cost of substantially slower RAM and register read/write times.

The bus interface is compatible with the two prevalent bus control signal methods: "Intel style" interface, characterized by separate strobes for read and write operations ($\overline{OE}$ and $\overline{WE}$), and "Motorola style" interface, characterized by a single read/write strobe ($\overline{STR}$) and a data direction signal (R/$\overline{W}$). Bus control style is selected using the BTYPE configuration pin, which sets the function of two other input pins to serve as either $\overline{OE}$ and $\overline{WE}$, or $\overline{STR}$ and R/$\overline{W}$.

The BWID configuration pin selects either 8- or 16-bit bus widths. When the BWID pin is connected to ground, 8-bit mode is selected; two bytes are sequentially transferred for each 16-bit word operation. The BENDI and A0 pins are used in conjunction with each other to define the byte order. When the BWID pin is connected high or left unconnected, 16-bit bus width is used and data is transacted on bus data pins D15:0. For 16-bit bus operation, the A0 pin is "Don't Care" and byte order is defined by the BENDI pin. The interoperability of BWID, BENDI and A0 pins is summarized in Table 4.

15.1.1. Bus Wait States and Data Prefetch

The HI-6120 has a WAIT output pin that tells the host to add wait states when additional access time is needed during bus read cycles. For compatibility with different host processors, the state of the WPOL input pin sets the WAIT output as active high or active low. The WAIT output can be ignored when the host processor read cycle time is always slow enough to work with the HI-6120 bus. When using fast host processors, cycle time is sometimes slowed down by configuring the processor to add one or more wait states during every read or write cycle, but slow-down affects all cycles, even when unnecessary.

Data prefetch is a technique used by the HI-6120 to speed up host multi-word read access to registers or RAM by eliminating wait states. Prefetching occurs when HI-6120 logic requests data before it is actually needed. Because register or RAM locations are often read sequentially, performance improves when data is prefetched in address sequence order. For every host read cycle, the device first reads the addressed location, then prefetches the following address, to speed up access in the likely event that the following word will be read next.

For the HI-6120, WAIT is always asserted for the first word fetched in any read sequence. The first read cycle has a long access time because there is no prefetch. This may be the first byte read in 8-bit mode, or the first word read in 16-bit mode. After each word (or byte) is fetched for a read operation, the next word (or byte) is prefetched to speed-up the read cycle time when sequential address read sequences occur. After the first word read, the following words read in sequence are accessed without WAIT, resulting in faster overall multi-word read timing. As long as bytes or words are read in address order, additional wait states are unnecessary.

Data prefetch during read cycles is blocked when the next RAM address is a Control Word in the Descriptor Table. The table base address (set by the value in register 0x0005) and every fourth word thereafter is a Control Word. This consists of table addresses having these address offsets from the table start address of 0, 4, 8, 0xC… 0x1F8 and 0x1FC. If allowed, prefetch (like any other read) would reset the Control Word DBAC status bit, so prefetch is disallowed in this range. Thus for HI-6120, **multi-word sequential read sequences will assert WAIT every fourth word when reading RAM within the 512-word Descriptor Table address range.**

For fastest read access under all conditions, the user can set host processor bus timing (by adjusting processor wait states for the chip select assigned to the HI-6120) to match the faster read cycle time for prefetched data, while the HI-6120 WAIT output adds one or more additional wait states for the slower initial read cycle.

Timing diagrams for bus read and write operations are shown in Section 17.5. Separate diagrams show "Intel style" and "Motorola style" control interfaces.

15.2. HI-6121 Serial Peripheral Interface

In the HI-6121, internal RAM and registers occupy a 32K x 16 address space. The lowest 32 addresses access registers and the remaining addresses access RAM locations. Timing is identical for register operations and RAM operations via the serial interface, and read and write operations have likewise identical timing.

15.2.1. Serial Peripheral Interface (SPI) Basics

The HI-6121 uses an SPI synchronous serial interface for host access to registers and RAM. Host serial communication is enabled through the Chip Enable ($\overline{CE}$) pin, and is accessed via a three-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host and Serial Clock (SCK). All programming cycles are completely self-timed, and no erase cycle is required before write.

The SPI (Serial Peripheral Interface) protocol specifies master and slave operation; the HI-6121 operates as an SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible “SPI Modes.” Without describing details of the SPI modes, the HI-6121 operates in the two modes where input data for each device (master and slave) is clocked on the rising edge of SCK, and output data for each device changes on the falling edge. These are known as SPI Mode 0 (CPHA = 0, CPOL = 0) and SPI Mode 3 (CPHA = 1, CPOL = 1). Be sure to set the host SPI logic for one of these modes.

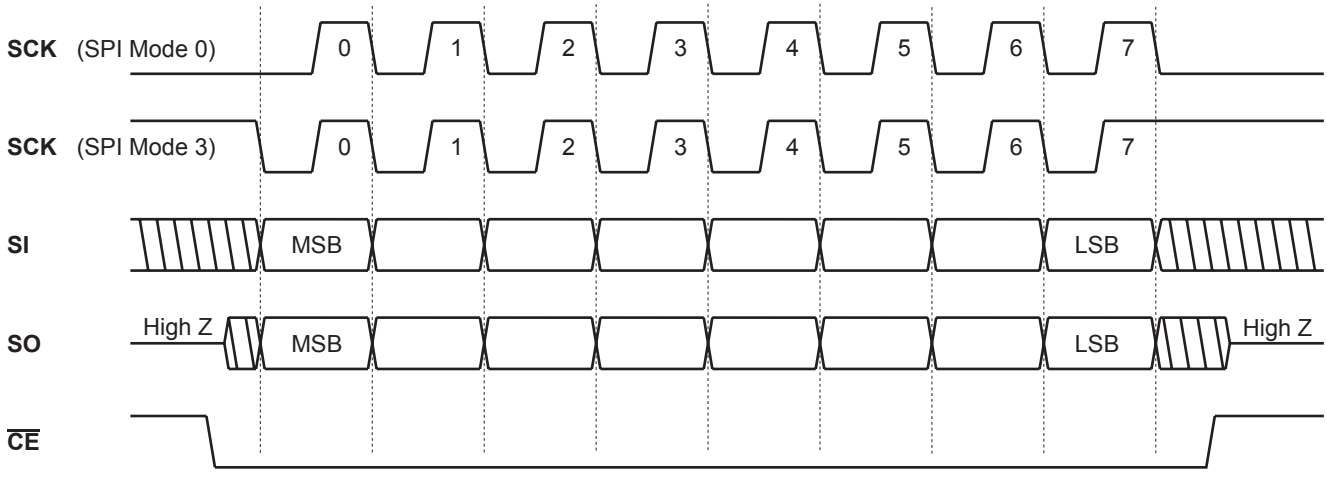


Figure 18. Generalized Single-Byte Transfer Using SPI Protocol. SCK is Shown for SPI Modes 0 and 3

The difference between SPI Modes 0 and 3 is the idle state for the SCK signal, which is logic 0 for Mode 0 state and logic 1 for Mode 3 state (see Figure 18). There is no configuration setting in the HI-6121 to select SPI Mode 0 or Mode 3 because compatibility is automatic. Beyond this point, the HI-6121 data sheet only shows the SPI Mode 0 SCK signal in timing diagrams.

The SPI protocol transfers serial data as 8-bit bytes. Once $\overline{CE}$ chip enable is asserted, the next 8 rising edges on SCK latch input data into the master and slave devices, starting with each byte's most-significant bit. The HI-6121 SPI can be clocked at 20 MHz.

Multiple bytes may be transferred when the host holds $\overline{CE}$ low after the first byte transferred, and continues to clock SCK in multiples of 8 clocks. A rising edge on $\overline{CE}$ chip enable terminates the serial transfer and reinitializes the HI-6121 SPI for the next transfer. If $\overline{CE}$ goes high before a full byte is clocked by SCK, the incomplete byte clocked into the device SI pin is discarded.

Two byte transfers are needed for SPI exchange of 16-bit register values or RAM data. See Bendi pin description in Section "2. Pin Descriptions" for details on setting byte order and "endianness".

In the general case, both master and slave simultaneously send and receive serial data (full duplex) per Figure 18 below. However the HI-6121 operates half duplex, maintaining high impedance on the SO output, except when actually transmitting serial data. When the HI-6121 is sending data on SO during read operations, activity on its SI input is ignored. Figure 19 and Figure 20 show actual behavior for the HI-6121 SO output.

15.2.2. HI-6121 SPI Commands

For the HI-6121, each SPI read or write operation begins with an 8-bit command byte transferred from the host to the device after assertion of $\overline{CE}$. Since HI-6121 command byte reception is half-duplex, the host discards the dummy byte it receives while serially transmitting the command byte.

The HI-6121 SPI command set uses the most significant command bit to specify whether the command is Read or Write. The command byte MSB is zero for read commands, and one for write commands.

15.2.3. Fast-Access Commands for Registers 0-15

The SPI command set includes directly-addressed read and write commands for registers 0 through 15. The 8-bit pattern for these commands has the general form

W-0-R-R-R-R-0-0

where RRRR is the 4-bit register address, and the most significant bit, W signifies Write when 1, or Read when 0. These fast-access commands appear in Table 14.

Figure 19 and Figure 20 show read and write timing as it appears for fast-access register operations. The command byte is immediately followed by two data bytes comprising the 16-bit data word read or written. For a register read or write, $\overline{CE}$ is negated after the 2-byte data word is transferred.

15.2.4. Indirect Addressing of RAM and Registers

Refer to the HI-6121 SPI command set shown in Table 15. SPI commands other than fast-access use an address pointer to indicate the address for read or write transactions. This "memory address pointer" resides at register address 15, and must be initialized before any read or write operation, other than fast-access.

To set the address pointer, use a fast-access write to register 15, consisting of command byte 0xBC followed by the desired 16-bit memory or register address. The pointer uses a 15-bit value to access any location in the 32K address range. The current address pointer value can be read using a fast-access read command byte 0x3C.

After a 2-byte read/write completion, the internal address pointer automatically increments to the following register address. The host can extend the read or write operation to the next register address by continuing to hold $\overline{CE}$ low while clocking SCK 16 additional times. This auto-increment feature can be used to access one or more sequential register addresses above the command address. Auto-increment applies (ranging to the top of the address space) as long as SCK continues to be clocked under continuous $\overline{CE}$ assertion. Caution: When the primary address pointer is used for auto-incrementing multi-word read/write and reaches the top of the address range (0x7FFF) the next increment will roll over the pointer value to 0x0000. The host should avoid this situation.

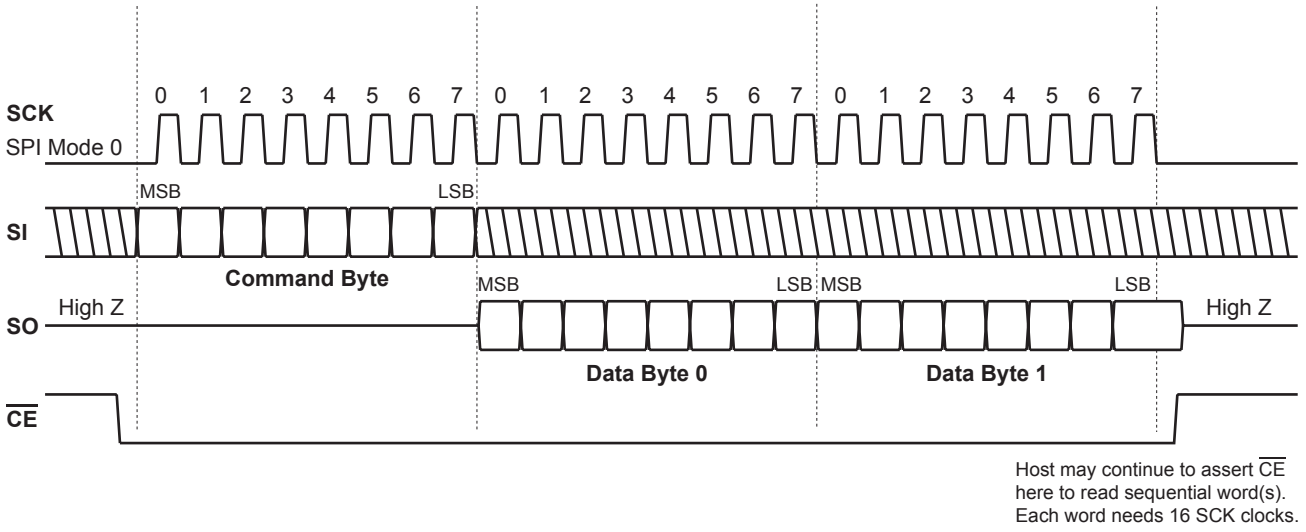


Figure 19. Single-Word (2-Byte) Read From RAM or a Register

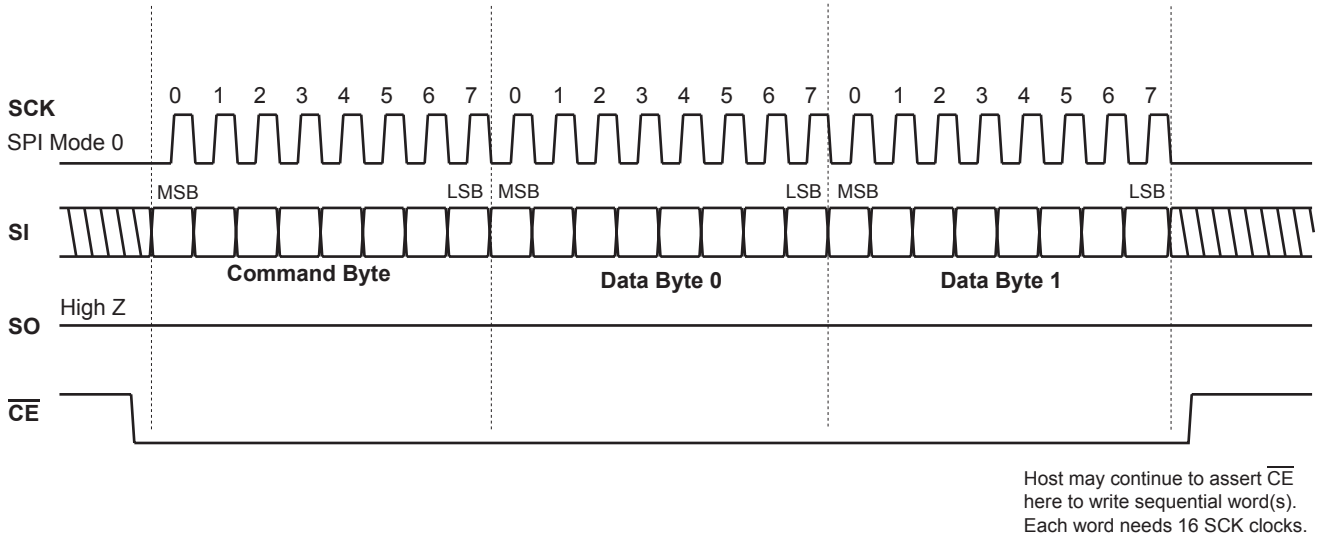


Figure 20. Single-Word (2-Byte) Write To RAM or a Register

Three single-byte SPI commands modify the current address pointer value in register 15:

Command	Address Pointer Operation
0xD0	add 1 to the current pointer value
0xD8	add 2 to the current pointer value
0xE0	add 4 to the current pointer value

The “Add 4” command may be useful when sequentially accessing the same word (for example, the Control Word) in a series of 4-word Descriptor Table entries. The “Add 2” command might be useful for reading the Interrupt Log Buffer, comprised of 2-word log entries. In both cases, the Add command would be probably followed by Read command 0x40 to read the location addressed by the current pointer value. Similarly, Write command 0xC0 writes the location addressed by the current pointer value. Two command bytes cannot be “chained”; $\overline{CE}$ must be negated after the Add command, then reasserted for the following Read or Write command.

The memory address pointer is not affected by fast-access read/writes to registers 0-14 because fast-access SPI commands use a separate, internal pointer not directly accessible to the host.

Just two single-byte SPI commands use the current address pointer value in register 15 without first loading or otherwise modifying it:

Command	Read Operation
0x40	read location addressed by pointer value

Command	Write Operation
0xC0	write location addressed by pointer value

Either of these commands can be used to read or write a single location, or may be used when starting a multi-word read or write by using the pointer’s auto-increment feature.

Two single-byte SPI commands increment the current address pointer value in register 15, then perform a read or write:

Command	Read Operation
0x48	add 1 to pointer then read addressed location

Command	Write Operation
0xC8	add 1 to pointer then write addressed location

15.2.5. Data Prefetch for SPI Read Cycles

Data prefetch is a technique used by the HI-6121 to speed up host multi-word read access to registers or RAM. Prefetching occurs when HI-6121 logic accesses data before it is actually needed. Because register or RAM locations are often read sequentially, performance improves when data is prefetched in address sequence order. For any SPI read cycle, the HI-6121 first fetches the addressed location, then increments the memory address pointer and prefetches the following address, to speed up access in the likely event that the following word will be read next. For the HI-6121, read cycle prefetch allows the SPI host to read sequential locations back-to-back, continuing as long as the host asserts chip select and provides SPI clock. This is described as the Memory Address Pointer “auto-increment” feature.

There is an exception: read cycle prefetch is blocked when the next RAM address is a Control Word in the Descriptor Table. If allowed, pre-fetch (like any other read) would reset the Control Word DBAC status bit. To preserve DBAC status bit function, prefetch is disabled when reading Control Words within Descriptor Table address range. The table base address (set by the value in register 0x0005) and every fourth word thereafter is a Control Word. This consists of table addresses having these offsets from the table start address: 0, 4, 8, 0xC through and including 0x1F8 and 0x1FC. See further information in Section 15.2.7.

These two commands can be used to read or write a single location, or may be used to start a multi-word read or write that uses the pointer’s auto-increment feature.

15.2.6. Special Purpose Commands

Several other HI-6121 SPI commands load or otherwise modify the primary address pointer before initiating a read or write process. These commands were tailored to the specific needs of HI-6121 Remote Terminal host software.

Using a single-byte SPI command, the address pointer can be directly loaded with the memory address for the descriptor table Control Word corresponding to the last completed MIL-STD-1553 command. The Control Word is then read.

Command	Read Operation
0x50	Copy Current Control Word Address register 13 to address pointer register 15. Read the location addressed by the new pointer value.

This command can be used to read just the current

Control Word, or may be used to start a multi-word read because memory pointer auto-increment occurs after the Control Word is read.

Six single-byte SPI commands add an offset to the current address pointer value, then read the addressed memory location; the read value is then written to the address pointer register 15. The new pointer value is used to start a read or write operation:

Command	Read Operation
0x68	Read the location addressed by the memory address pointer. Write the value just read into the memory address pointer. Then read.
0x70	Add 1 to the memory address pointer. Read value at newly addressed location and write it into the memory address pointer. Then read.
0x78	Add 2 to the memory address pointer. Read value at newly addressed location and write it into the memory address pointer. Then read.

Command	Write Operation
0xE8	Read the location addressed by the memory address pointer. Write the value just read into the memory address pointer. Then write.
0xF0	Add 1 to the memory address pointer. Read value at newly addressed location and write it into the memory address pointer. Then write.
0xF8	Add 2 to the memory address pointer. Read value at newly addressed location and write it into the memory address pointer. Then write.

Primary use occurs when a Descriptor Table Control Word was just read. For example, the last op code performed was 0x50, reading the Control Word for the last command. After reading the Control Word, the memory pointer has automatically incremented. The host can examine flag bits contained in the just-read Control Word to determine the applicable data buffer (e.g., Data Buffer A, Data Buffer B or the Broadcast Data Buffer) then directly service that buffer using these op codes; the three data buffer pointers occur in the three words following the initially read Control Word.

These six commands can be used to read or write a single location, or may be used to start a multi-word read or write that uses the pointer's auto-increment feature.

When some or all subaddress or mode commands are not programmed to trigger host interrupts, a different single-byte SPI command may be useful if polling the Descriptor Table for message activity. In this situation, the host may poll a series of Descriptor Table Control Words looking for instances where the DBAC activity bit is set. The DBAC (Descriptor Block Accessed) flag is set in the Control Word each time the corresponding command is completed. The process of reading the Control Word automatically resets the register's DBAC bit so the host can detect activity the next time the DBAC flag is set by the device.

Since Descriptor Table Control Words are spaced four words apart, this command is useful when polling a series of descriptor table Control Words:

Command	Read Operation
0x60	Read addressed location then add 4 to pointer

Primary use occurs when the address pointer initially points to the first Descriptor Table Control Word in a series of Control Words to be polled (every fourth word).

After 8 SCK clocks for the SPI command, each instance of this command reads a single location using 16 SCK clocks. If $\overline{CS}$ remains low after 24 clocks and SCK continues, a multi-word read begins, using the address pointer's auto-increment feature. The second word read is at (Control Word address + 4), the next Control Word in the table. As long as $\overline{CS}$ remains continuously asserted and the host SPI continues SCK clock, every fourth word will be read from memory. Once $\overline{CS}$ goes high at the end of a multi-word read sequence, the memory address pointer will contain (Last Read Address + 3). When necessary to resume reading every fourth address, the host can issue SPI op code 0xD0 to increment the address pointer, before reissuing op code 0x60. A new multi-word sequence begins, starting with the next address in the read-by-4 series.

Another single-byte SPI command is useful when servicing interrupts. When enabled interrupts occur, two words are written to the circular 32-word Interrupt Log Buffer, and the Interrupt Log Address register 9 is updated to show the storage address where interrupt information words will be stored for the next occurring interrupt. Buffer starting address is 0x0040 and ending address is 0x005F. Because two words are written to the buffer for each interrupt, the Interrupt Log Address register always contains an even value in the range of 0x0040 to 0x005E.

When servicing an interrupt that just occurred, the host wants timely information on that interrupt. An SPI com-

mand is provided to simplify interrupt handling:

Command	Read Operation
0x58	Write memory address pointer 0x000F with address of last-written Interrupt Address Word in the Interrupt Log. Read the addressed RAM location (IAW) then decrement address pointer to point to the corresponding Interrupt Information Word (IIW). As long as $\overline{CS}$ remains continuously asserted and the host SPI continues SCK clock, successive read and decrement cycles read out Interrupt Log words in LIFO (Last-In First-Out) order, automatically wrapping around the log's 0x0040 to 0x005F address range.

This command is used when starting a multi-word read from the Interrupt Log. The memory address pointer automatically decrements after each word read, automatically wrapping around the log's 0x0040 to 0x005F address range. This is the only SPI op code that decrements the memory pointer for multi-word operations. The first word read is always the last-written IAW, so the log data is read in LIFO order, as long as $\overline{CS}$ remains continuously asserted and the host SPI continues SCK. Once $\overline{CS}$ goes high at the end of a multi-word read sequence, the memory address pointer value is indeterminate.

15.2.7. Descriptor Table Prefetch Exceptions

For the SPI-interface HI-6121, the Memory Address Pointer (register 0x000F) contains the address for each new word read by the host. When starting a read access, the host usually writes the memory address pointer with the address for the first word to read. The host then uses an SPI op code to initiate the read process. After the addressed word is transferred by SPI to the host, the HI-6121 continues to read and transmit words from sequential RAM memory addresses, as long as the host continuously asserts chip select while providing SCK serial clock pulses. After fetching each new word, the device increments the Memory Address Pointer and prefetches the data contained in the newly addressed location. The next word is prefetched even when the host does not ultimately read the following address. **For HI-6121, sequential reads from Descriptor Table that rely on MAP auto-increment will stop advancing when the next address contains a table Control Word.** Properly designed SPI transfers overcome this behavior.

Using SPI command op codes, the HI-6121 host must consider prefetch and pointer behavior when reading data from the Descriptor Table. Applied outside the Descriptor Table, the following SPI sequence would read data from six successive memory addresses. But below, applied within the table, the sequence gets stuck at the fourth word read.

Here we assume the Descriptor Table starts at default base address, 0x0200. The host first uses SPI op code 0xBC to store the table start address 0x0200 in the Memory Address Pointer, then uses op code 0x40 (and MAP auto-increment) to read the MAP-addressed location and successive locations.

Notice: There is no MAP auto-increment or data prefetch when MAP equals 0x0203, so the final two read cycles repeat the previous read value and address.

```
FROM    FROM
HOST    HI-6121   COMMENT
=====   =======   ========================================
0xBC     ----     SPI op code writes memory address pointer (MAP).
0x0200   ----     The table start address written to MAP.
0x40     ----     SPI op code to "read location addressed by MAP"
----    <data>    data from 0x0200 (SCK continues afterward)
----    <data>    data from 0x0201 (SCK continues afterward)
----    <data>    data from 0x0202 (SCK continues afterward)
----    <data>    data from 0x0203 (SCK continues afterward, Control Word next)
----    <data>    data from 0x0203 (SCK continues afterward, Control Word next)
----    <data>    data from 0x0203 (SCK stops and /CS is then negated)
```

Using a different SPI op code, the host can sequentially read the entire Descriptor Table.

```
FROM   FROM
HOST   HI-6121  COMMENT
=====  =======  ========================================
0xBC    ----    op code writes memory address pointer (MAP)
0x01FF  ----    decremented table start addr 0x0200 - 1 written to MAP

0x48    ----    op code pre-increment MAP then read addressed location
----   <data>   data from 0x0200 (SCK continues afterward)
----   <data>   data from 0x0201 (SCK continues afterward)
----   <data>   data from 0x0202 (SCK continues afterward)
----   <data>   data from 0x0203 (SCK stops and /CS is negated)

0x48    ----    op code pre-increment MAP then read addressed location
----   <data>   data from 0x0204 (SCK continues afterward)
----   <data>   data from 0x0205 (SCK continues afterward)
----   <data>   data from 0x0206 (SCK continues afterward)
----   <data>   data from 0x0207 (SCK stops and /CS is negated)

0x48    ----    op code pre-increment MAP then read addressed location
----   <data>   data from 0x0208 (SCK continues afterward)
----   <data>   data from 0x0209 (SCK continues afterward)
----   <data>   data from 0x020A (SCK continues afterward)
----   <data>   data from 0x020B (SCK stops and /CS is negated)
```

The host may repeat this sequence until the entire Descriptor Table is read. The repeating read process is not shown, but the sequence could end like this, continuing beyond the table boundary…

```
0x48    ----    op code pre-increment MAP then read addressed location
----   <data>   data from 0x03FC (SCK continues afterward)
----   <data>   data from 0x03FD (SCK continues afterward)
----   <data>   data from 0x03FE (SCK continues afterward)
----   <data>   data from 0x03FF (SCK continues afterward) TABLE ENDS
```

Table 14. Fast-Access SPI Commands for Registers 0-15

Command Bits 5:2 Convey the 4-Bit Register Address.

Command Bits 7 6 5 4 3 2 1 0	HEX Byte	Fast-Access Read	Command Bits 7 6 5 4 3 2 1 0	HEX Byte	Fast-Access Write
0 0 0 0 0 0 0 0	0x00	Read Register 0	1 0 0 0 0 0 0 0	0x80	Write Register 0
0 0 0 0 0 1 0 0	0x04	Read Register 1	1 0 0 0 0 1 0 0	0x84	Write Register 1
0 0 0 0 1 0 0 0	0x08	Read Register 2	1 0 0 0 1 0 0 0	0x88	Write Register 2
0 0 0 0 1 1 0 0	0x0C	Read Register 3	1 0 0 0 1 1 0 0	0x8C	Write Register 3
0 0 0 1 0 0 0 0	0x10	Read Register 4	1 0 0 1 0 0 0 0	0x90	Write Register 4
0 0 0 1 0 1 0 0	0x14	Read Register 5	1 0 0 1 0 1 0 0	0x94	Write Register 5
0 0 0 1 1 0 0 0	0x18	Read Register 6	1 0 0 1 1 0 0 0	0x98	Write Register 6
0 0 0 1 1 1 0 0	0x1C	Read Register 7	1 0 0 1 1 1 0 0	0x9C	Write Register 7
0 0 1 0 0 0 0 0	0x20	Read Register 8	1 0 1 0 0 0 0 0	0xA0	Write Register 8
0 0 1 0 0 1 0 0	0x24	Read Register 9	1 0 1 0 0 1 0 0	0xA4	Write Register 9
0 0 1 0 1 0 0 0	0x28	Read Register 10	1 0 1 0 1 0 0 0	0xA8	Write Register 10
0 0 1 0 1 1 0 0	0x2C	Read Register 11	1 0 1 0 1 1 0 0	0xAC	Write Register 11
0 0 1 1 0 0 0 0	0x30	Read Register 12	1 0 1 1 0 0 0 0	0xB0	Write Register 12
0 0 1 1 0 1 0 0	0x34	Read Register 13	1 0 1 1 0 1 0 0	0xB4	Write Register 13
0 0 1 1 1 0 0 0	0x38	Read Register 14	1 0 1 1 1 0 0 0	0xB8	Write Register 14
0 0 1 1 1 1 0 0	0x3C	Read Register 15	1 0 1 1 1 1 0 0	0xBC	Write Register 15

Table 15. SPI Commands using Address Pointer Register

Hex Byte	Read or Write	Read
Address Pointer Operations (no data is written or read, no pointer auto-increment)		
0xD0	-------	Add 1 to the current address pointer value in register 15
0xD8	-------	Add 2 to the current address pointer value in register 15
0xE0	-------	Add 4 to the current address pointer value in register 15
Read / Write RAM or Register Location Using Current Address Pointer Value		
0x40	R	Read location addressed by current address pointer value in register 15
0xC0	W	Write location addressed by current address pointer value in register 15
Increment Address Pointer Then Read / Write Addressed RAM or Register Location		
0x48	R	Read addressed location after incrementing pointer in register 15
0xC8	W	Write addressed location after incrementing pointer in register 15
Special Purpose Commands		
0x50	R	Copy register 13 (current Control Word address) to address pointer in register 15, then read the location addressed by the new pointer value (read the current Control Word)
0x68	R	Add 0 to the current address pointer value in register 15. Then . . .
0x70	R	Add 1 to the current address pointer value in register 15. Then . . .
0x78	R	Add 2 to the current address pointer value in register 15. Then copy value from newly addressed location to address pointer in register 15 then read newly addressed location.
0xE8	W	Add 0 to the current address pointer value in register 15. Then . . .
0xF0	W	Add 1 to the current address pointer value in register 15. Then . . .
0xF8	W	Add 2 to the current address pointer value in register 15. Then copy value from newly addressed location to address pointer in register 15 then write newly addressed location.
0x60	R	Read then add 4 to the address pointer value in register 15 (multi-word reads only).
0x58	R	Write storage address of last-written Interrupt Address Word to the address pointer in register 15. Read IAW from Interrupt Log buffer, then decrement address pointer. Uninterrupted multi-word read cycles fetch words from the Interrupt Log in LIFO order.

16. APPENDIX: RT MESSAGES RESPONSES, OPTIONS & EXCEPTIONS

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Invalid Command Word (Manchester, parity or bit count error)	No terminal response, the message is ignored. No Status Word change.	No change	No Message Info Word is written	None
Any valid command to RT31 (broadcast). when the BCSTINV bit in Configuration Register 1 equals 1.	No terminal response, the message is ignored. No Status Word change. (Broadcast commands are rendered invalid.)	No change	No Message Info Word is written	None
RT Address Parity Error based on RTA and RTAP bits in the Operational Status Register	For commands to the RT's own address or to broadcast address RT31: No terminal response, message is ignored. No Status Word change.	No change	No Message Info Word is written	RTAPF (not optional)
Any valid non-mode (subaddress 1-30) transmit command to RT31 (undefined broadcast transmit).	No terminal response, Set Message Error (ME) and BCR status bits.	DBAC bit set. DPB bit toggles. BCAST bit set.	MERR bit set. BUSID bit updated.	IWA IBR (IXEQZ)
Any valid non-mode (subaddress 1-30) transmit command except for RT31. The corresponding bit in the Illegalization Table equals 0.*	Normal Status Word response (Clear Status). Data words for transmit are read from the RAM data buffer assigned by the Descriptor Table entry for the transmit subaddress.	DBAC bit set. DPB bit toggles. BCAST bit reset.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (Other error bits reset).	IWA IBR (IXEQZ)
Any valid non-mode (subaddress 1-30) transmit command except for RT31. The corresponding bit in the Illegalization Table equals 1. **	Assert Message Error (ME) status, then transmit ME Status Word without following data words.	DBAC bit set. DPB bit toggles. BCAST bit reset.	ILCMD bit set. BUSID bit updated. MERR bit set. RTRT bit updated. (Other error bits reset).	ILCMD IWA
Any valid non-mode (subaddress 1-30) receive command. The corresponding bit in the Illegalization Table equals 0. *	Normal Status Word response (Clear Status). After message completion, the data words received are stored in the data buffer RAM location assigned by the Descriptor Table entry for the receive subaddress.	DBAC bit set. DPB bit toggles. BCAST bit reset.	Normal update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (Other error bits reset).	IWA IBR (IXEQZ)

* Terminal is using "illegal command detection" and command is legal
OR terminal is not using "illegal command detection" and command may be legal or illegal (in form response).
** Terminal is using "illegal command detection" and command is illegal.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Any valid non-mode (subaddress 1-30) receive command. The corresponding bit in the Illegalization Table equals 1. **	Assert Message Error (ME) status and set BCR if broadcast. Any received data words are ignored and are not saved. When data reception stops, transmit Status Word.	DBAC bit set. DPB bit toggles. BCAST bit updated.	ILCMD bit set. BUSID bit updated. MERR bit set. RTRT bit updated. (Other error bits reset)	ILCMD IWA IBR (IXEQZ)
Valid receive command followed by invalid data word (Manchester, parity or bit count error).	No terminal response. Set Message Error (ME) status. If broadcast (RT31), also set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. IWDERR bit set. ILCMD bit reset. RTRT bit updated (Other error bits reset).	MERR IWA IBR
Valid receive command followed by one or more good data words, then a data word having Command Sync.	No terminal response. Set Message Error (ME) status. If broadcast (RT31), also set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. SYNERR bit set. ILCMD bit reset. (Other error bits reset).	MERR IWA IBR
Any valid command followed by wrong number of data words (too few or too many words)	No terminal response. Set Message Error (ME) status. If broadcast (RT31), also set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. Set WCTERR (too few) or GAPERR (too many). ILCMD bit reset. RTRT bit updated. (Other error bits reset).	MERR IWA IBR
RT-RT where CW1 is a valid non-mode receive command. CW2 is a non-mode transmit command valid for different RT. (Normal RT-RT receive message)	Normal Status Word response (Clear Status). If RT-RT Command Word 1 is broadcast (RT31) set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. RTRT bit set. RTCWERR bit reset. ILCMD bit reset. (All error bits reset).	IWA IBR (IXEQZ)
RT-RT where CW1 is a valid non-mode receive command. Transmit command CW2 has an error: T/$\overline{R}$ bit = 0, or CW2 subaddress equals 0 or 31 (mode code), or CW2 has same RT address as CW1.	No terminal response. Set Message Error (ME) status. If RT-RT Command Word 1 is broadcast (RT31) also set the BCR status bit,	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. RTRT bit set. RTRTCWERR bit set. ILCMD bit reset. (Other error bits reset).	MERR IWA IBR

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
RT-RT where CW1 is a valid non-mode receive command. CW2 is valid for different RT but transmitting RT does not respond in time.	No terminal response. Set Message Error (ME) status. If RT-RT Command Word 1 is broadcast (RT31), also set the BCR status bit.	DBAC bit set. BCAST bit updated DPB bit toggles.	MERR bit set. BUSID bit updated. RTRT bit set. TMOERR bit set. ILCMD bit reset. (Other error bits reset).	MERR IWA IBR
RT-RT receive command (CW1 is valid). The transmitting RT response has one of these errors: invalid word (Manchester, (sync, bit count, parity or word count error). Also includes transmitting RT response with Message Error or Busy status followed by no data words.	No terminal response. Set Message Error (ME) status. If RT-RT Command Word 1 is broadcast (RT31) also set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. BUISID bit reset. RTRT bit set. IWDERR bit set, or WCTERR bit set for Tx RT Busy case. ILCMD bit reset. (Other error bits reset).	MERR IWA IBR
RT-RT command where CW2 is a valid non-mode (subaddress 1-30) transmit command. CW1 is a non-mode receive command for RT31. (Normal broadcast RT-RT transmit)	Normal Status Word response. Clear status is transmitted with the commanded number of data words. Data words for transmit are read from the RAM data buffer assigned in the Descriptor Table entry for the transmit subaddress.	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit set. (All error bits reset).	IWA (IXEQZ)
Valid mode code command to RT31 (broadcast). The BCSTINV bit in Configuration Register 1 equals 1.	No terminal response, the message is ignored. No Status Word change.	No change	No Message Info Word is written	None
Valid undefined mode code command. The UMCINV bit in Configuration Register 1 equals 1.	No terminal response, the message is ignored. No Status Word change. **NOTE:** This only applies for the undefined mode codes: MC0 to MC15 with T/$\overline{R}$ = 0 MC16,18 & 19 with T/$\overline{R}$ = 0 MC17,20 & 21 with T/$\overline{R}$ = 1	No change	No Message Info Word is written	None

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Valid defined mode code command (including reserved mode code) not "illegalized" by Illegalization Table (table bit equals 0 *)	If MC2 (transmit status) or MC18 (transmit last command) status word from last command is transmitted. If MC18, data word transmitted is read from an internal register. **OR** If not MC2 or MC18, normal Status Word response. If broadcast, assert Status Word BCR bit. For mode codes 16-31 with T/$\overline{R}$ bit = 1 which transmit a data word, the word for transmit is read from the Mode Command Data Table. **AND** For all mode commands with mode data word (mode codes 16-31), the transmitted or received data word is written to command's Descriptor Word 4.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR (IXEQZ)
Valid defined mode code command that is "illegalized" by the IllegalizationTable (table bit equals 1 **)	Set Message Error (ME) status. If not broadcast (RT31), transmit. Status Word without a following mode data word. If broadcast (RT31), also assert the BCR status bit. **AND** For mode commands with a mode data word (mode codes 16-31), no updates are made to the Mode Command Data Table or to the command's Word 4 in Descriptor Table.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. BUSID bit updated. MERR bit reset. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR

* Terminal is using "illegal command detection" and command is legal
OR terminal is not using "illegal command detection" and command may be legal or illegal (in form response).
** Terminal is using "illegal command detection" and command is illegal.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Valid undefined mode code command. The UMCINV bit in Configuration Register 1 equals 0.	If bit in Illegalization Table that corresponds to the undefined mode code command equals 1 ** Set Message Error (ME) status, If not broadcast (RT31), transmit Status Word without a following mode data word. If broadcast (RT31), also assert the BCR status bit. **OR** If bit in Illegalization Table that corresponds to the undefined mode code command equals 0 * Normal Status Word (Clear Status) response. If command was broadcast (RT31), assert the BCR status bit. **AND** For mode codes 16-31 with T/$\overline{R}$ bit = 1 which transmit a data word, the word for transmit is read from the Mode Command Data Table. **AND** For all mode commands with mode data word (mode codes 16-31), the transmitted or received data word is written to command's Descriptor Word 4.	DBAC bit set. BCAST bit updated. DPB bit toggles. DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. BUSID bit updated. MERR bit reset. RTRT bit reset. (Other error bits reset.) Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	ILCMD IWA IBR IWA IBR (IXEQZ)

* Terminal is using "illegal command detection" and command is legal
OR terminal is not using "illegal command detection" and command may be legal or illegal (in form response).
** Terminal is using "illegal command detection" and command is illegal.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
Valid receive command followed by invalid data word (Manchester, parity or bit count error).	No terminal response. Set Status Word ME bit, If broadcast, also set Status Word BCR bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. BUSID bit updated. IWDERR bit set. ILCMD bit reset. RTRT bit updated. (Other error bits reset.)	MERR IWA IBR
Superseded Message: Terminal receives an incomplete message interrupted by a gap of at least 3.5 us, followed by a new valid command on the same bus or on the other bus **OR** Terminal is transacting a transmit message on one bus and receives the start of a valid command on the other bus.	Terminal aborts processing for first message and responds in full to the second (superseding) message. The Status Word BCR bit reflects broadcast status for: the second command, unless second command is MC2 (transmit status) or MC18 (transmit last command).	No change to superseded command's Control Word. For superseding command's Control Word: DBAC bit set. BCAST bit updated DPB bit toggles.	No Msg Info Word written for the superseded command. For superseding command's data buffer, a normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (All error bits reset.)	None for super-seded command IWA IBR (IXEQZ)
Terminal is Busy for a valid receive command either globally (BUSY bit set in Status Word Bits register) or in response to a particular valid receive command (MKBUSY bit set in the command's Descriptor Table control word.)	Busy bit is set in the 1553 Status Bits register. Status Word is transmitted, unless broadcast. If broadcast, the BCR bit in Status Word is also set. After message completion, data words received are stored in the data buffer assigned by the receive subaddress Descriptor Table entry.	DBAC bit set. BCAST bit updated. DPB bit toggles.	WASBSY bit set. BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (All error bits reset.)	IWA IBR
Terminal is Busy for a valid transmit command either globally (BUSY bit set in Status Word Bits register) or in response to a particular valid receive command (MKBUSY bit set in the command's Descriptor Table control word.)	Busy bit is set in the 1553 Status Bits register. If not broadcast, Status Word is transmitted without data. If broadcast, the BCR bit in Status Word is also set.	DBAC bit set. BCAST bit updated, (mode commands with T/$\overline{R}$ = 1) DPB bit toggles	WASBSY bit set. BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit updated. (All error bits reset.)	IWA IBR

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
DYNAMIC BUS CONTROL (MC0): Mode code command with mode code 00000 and T/$\overline{R}$ bit equals 1	HI-6110 is not equipped to accept bus control duties. The host must initialize device to respond using either of the two following methods:			
The mode code's bit in Illegalization Table equals 0 *	RT is not using "illegal command detection." Respond "in form": Reset Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
OR The mode code's bit in Illegalization Table equals 1 **	**OR** RT is using "illegal command detection"and mode code is illegalized. Set Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit reset. DPB bit toggles.	ILCMD bit set. BUSID bit updated. MERR bit reset. RTRT bit reset. (Other error bits reset.)	ILCMD IWA
MC0 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (MC0 is not ndefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None

* Command is illegal but terminal is not using "illegal command detection" (in form response).
** Command is illegal and terminal is using "illegal command detection"
*** Undefined mode command rendered invalid by UMCINV option bit. Command's bit in Illegalization Table is "don't care".

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 0. Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 0. Illegalization Table bit equals 1 **	Set Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit reset. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
SYNCHRONIZE WITHOUT DATA (MC1): Mode code command with mode code 00001 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress Status Word transmit. Reset the Time Tag counter to 0x0000.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
MC1 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response. The Time Tag counter is not reset.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response. The Time Tag counter is not reset.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”
*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMIT STATUS (MC2): Mode code command with mode code 00010 and T/$\overline{R}$ bit equals 1	No Status Word updates, Transmit Status from last valid command (assuming last command was not a "Transmit Status" or a "Transmit last Command" mode command.	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
MC2 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB bit toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0 The Illegalization Table bit equals 0 *	Respond "In form": Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response. Time Tag counter is not reset.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0 The Illegalization Table. bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

* Command is illegal but terminal is not using "illegal command detection" (in form response).
** Command is illegal and terminal is using "illegal command detection"
*** Undefined mode command rendered invalid by UMCINV option bit. Command's bit in Illegalization Table is "don't care".

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
INITIATE SELF TEST (MC3): Mode code command with mode code 00011 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress status transmit. Host should initiate self-test then update Built-In Test word at shared RAM address 0x0093. Resume terminal execution.	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
MC3 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”
*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMITTER SHUTDOWN (MC4): Mode code command with mode code 00100 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set Status Word BCR bit and suppress status. transmit. After Status transmission, inhibit the inactive bus:	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
The device automatically shuts down either **transmit and receive** or **transmit only** for the inactive bus, depending on the state of the SDSEL bit in Configuration Register 2. (See description of SDSEL and MCOPT4 bits in Configuration Register 2 for further information. When a bus transmitter (or transmitter and receiver) is shut down by mode command, bus status is reflected by assertion of a TXASD or TXBSD bit in the Built-In Test Register at register address 0x0014. If SDSEL equals logic 0, an RXASD or RXBSD bit will also be asserted. See Built-In Test Register description for further information. Once shutdown, the inactive bus transmitter (or transmitter and receiver can only be reactivated by an “Override Transmitter Shutdown” MC5 or MC21 or “Reset Remote Terminal” MC8 mode code command, or by software reset (by setting the SRST bit in Configuration Register 1) or by hardware reset initiated by asserting the MR master reset input pin.				
MC4 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”
*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
OVERRIDE TRANSMITTER SHUTDOWN (MC5): Mode code command with mode code 00101 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress status transmit. This command is only used with dual redundant buses. After Status transmission, reactivate inactive bus:	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
The device automatically re-enables **transmit and receive** for the inactive bus, regardless of the state of the SDSEL bit in Configuration Register 2. The device affirms reenabled bus status by resetting all four TXASD, TXBSD, RXASD and/or RXBSD bits in the Built-In Test Register at register address 0x0014. Note: If the TXINHA or TXINHB input pins are asserted, the device cannot override the resulting hardware transmit inhibit for the affected bus. In this case, the corresponding TXASD and/or TXBSD bits remain high. See Built-In Test Register description for further information.				
MC5 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”
*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
INHIBIT TERMINAL FLAG BIT (MC6): Mode code command with mode code 00110 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress status transmit.	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
The device automatically sets the TF Inhibit bit in the BIT Word register at address 0x0013. While the TF inhibit bit is set, the device disregards assertion of the Terminal Flag (TF) bit in the 1553 Status Bits register (0x0006) and only transmits status with the Terminal Flag status bit reset. Once the Terminal Flag has been inhibited, it can be reactivated by an "Override Inhibit Terminal Flag" MC7 or "Reset Remote Terminal" MC8 mode command, by software reset (asserting the SRST bit in Configuration Register 1) or by asserting the $\overline{MR}$ master reset input pin.				
MC6 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond "In form": Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
OVERRIDE INHIBIT TERMINAL FLAG BIT (MC7): Mode code command with mode code 00111 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status then transmit Status Word. If broadcast, set the Status Word BCR bit and suppress status transmit.	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
The device automatically resets the TF Inhibit bit in the BIT Word register at address 0x0013. While the TF inhibit bit is reset, the device transmits status with the Terminal Flag status bit set if the Terminal Flag (TF) bit is asserted in the 1553 Status Bits register (0x0006).				
MC7 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
RESET REMOTE TERMINAL (MC8): Mode code command with mode code 01000 and T/$\overline{R}$ bit equals 1	Default response: Reset Message Error (ME) status. If not broadcast, transmit Status Word.	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA IBR
After Status transmission, the device automatically resets the status Message Error (ME) Busy and Broadcast Command received (BCR) bits in its internal status register. The BIT Word at shared RAM address is reset to 0x0000. If either transmitter was shutdown, the shutdown condition is overridden. If the Terminal Flag (TF) status bit was inhibited, the inhibit is reset. This command does not reset any of the host-programmed registers that configure the terminal for operation. To complete the terminal reset process, the host must assert either MR hardware master reset (with or without auto-initialization) or assert the SRST bit in Configuration Register 1 to execute software reset. See following section entitled Reset and Initialization for additional details. Because MC8 requires host interaction, most applications will probably utilize the IWA interrupt to alert the host when received.				
MC8 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. GAPERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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** Command is illegal and terminal is using “illegal command detection”
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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
RESERVED MODE CODES MC9 - MC15: Mode code command with mode codes 01001 through 01111 and T/$\overline{R}$ bit equals 1	The reserved mode code commands do not have defined terminal actions. Host must initialize device to respond using either of the two following methods:			
The mode code's bit in Illegalization Table equals 0 *	RT is not using "illegal command detection." Respond "in form": Reset Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit reset. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
OR The mode code's bit in Illegalization Table equals 1 **	**OR** RT is using "illegal command detection"and mode code is illegalized. Set Message Error (ME) status and transmit Status Word.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. BUSID bit updated. MERR bit set. RTRT bit reset. (Other error bits reset.)	ILCMD IWA
MC9 - MC15 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond "In form": Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMIT VECTOR WORD (MC16): Mode code command with mode code 10000 and T/$\overline{R}$ bit equals 1	Default CS response: Reset Message Error (ME) and BCR status bits. then transmit Status Word followed by the data word stored in the assigned index or ping-pong data buffer (or in Descriptor Word 4 for SMCP Simplified Mode Command Processing).	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
MC16 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
SYNCHRONIZE WITH DATA WORD (MC17): Mode code command with mode code 10001 and T/$\overline{R}$ bit equals 0	Default response: Reset Message Error (ME) status. and transmit Status Word. If broadcast, set BCR status bit and suppress Status response.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
Device stores received data word in the assigned ping-pong or index data buffer (or in Descriptor Word 4 for SMCP Simplified Mode Command Processing). Configuration Register 2 MCOPT2 and MCOPT3 bits allow automatic Time-Tag count loading using the data word received. If MCOPT2 equals 1, the received data word is automatically loaded to the Time-Tag counter if the low order bit of the received data word (bit 0) equals 0. If MCOPT3 equals 1, the received data word is automatically loaded to the Time-Tag counter if the low order bit of the received data word (bit 0) equals 1. If both bits are set, the received data word is unconditionally loaded into the Time-Tag counter. For non-broadcast commands, counter load occurs before status word transmission.				
MC17 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 1 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 1)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 1 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 1 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word not followed by a contiguous data word (missing data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Mode code command word followed by data word with Manchester encoding or parity error (bad data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. IWDERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMIT LAST COMMAND (MC18): Mode code command with mode code 10010 and T/$\overline{R}$ bit equals 1	Default response: Status is not updated. Transmit Status Word from the previous command, with data word containing the last valid command word (assuming it was not a “Transmit Status” or a “Transmit Last Command” mode command.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
Transmitted data word is automatically provided from an internal register, and is copied to assigned index or ping-pong buffer (or to Descriptor Word 4 for SMCP Simplified Mode Command Processing)				
MC18 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
TRANSMIT BIT WORD (MC19): **Mode code command with mode code 10011** **and T/$\overline{R}$ bit equals 1**	Default response: Reset Message Error (ME) and BCR status bits. then transmit Status Word followed by data word from either BIT Word Register or Alternate BIT Word Register, depending on Configuration Reg. 2 option bit ALTBITW.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit reset. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
Transmitted data word is automatically copied to the assigned index or ping-pong buffer (or to Descriptor Word 4 for SMCP Simplified Mode Command Processing)				
MC19 EXCEPTIONS:				
Broadcast address RT31 (broadcast not allowed)	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB toggles.	MERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Invalid command word. **OR** T/$\overline{R}$ bit equals 0 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 0)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 0 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

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Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
SELECTED TRANSMITTER SHUTDOWN (MC20): Mode code command with mode code 10100 and T/$\overline{R}$ bit equals 0	Default response: Reset Message Error (ME) status. and transmit Status Word. If broadcast, set BCR status bit and suppress Status response. This command is intended for use in 1553 systems with more than one dual redundant bus.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA

After Status Word transmission, the device stores received data word in the assigned index or ping-pong buffer (or in Descriptor Word 4 if SMCP Simplified Mode Command Processing applies).

If the MCOPT4 bit in Configuration Register 2 equals 0, the received data word is compared to the value in the Bus Select Register corresponding to the inactive bus. For example, if the command is received on Bus A, the comparison uses the Bus B Select Register value. If the compared values match, the device automatically shuts down either **transmit and receive** or **transmit only** for the inactive bus, depending on the state of the SDSEL bit in Configuration Register 2. (See description of SDSEL and MCOPT4 bits in Configuration Register 2 for further information. When a bus transmitter (or transmitter and receiver) is shut down by this mode command, bus status is reflected by assertion of a TXASD or TXBSD bit in the Built-In Test Register at register address 0x0014. If SDSEL equals logic 0, an RXASD or RXBSD bit will also be asserted. See Built-In Test Register description for further information.

If MCOPT4 bit in Configuration Register 2 equals 0, the IWA interrupt is typically used to alert the host when an MC20 command is received. **The host** must evaluate whether the received mode data word matches the bus selection criteria. If bus selection criteria is met, **the host** fulfills bus shutdown command using one of two options:

1. set the bus shutdown bit INHBUSA or INHBUSB for the inactive bus in Configuration Register 1 **to inhibit both transmit and receive,**

OR

2. assert the transmit shutdown input pin TXINHA or TXINHB for the inactive **bus to inhibit only transmit.** The inactive bus receiver is still active and all valid commands are heeded without transmit. **This option is rarely applied.**

Once shutdown, the inactive bus transmitter (or transmitter and receiver) can only be reactivated by an “Override Transmitter Shutdown” MC5 or MC21 or “Reset Remote Terminal” MC8 mode code command, or by software reset (by setting the SRST bit in Configuration Register 1) or by hardware reset initiated by asserting the $\overline{MR}$ master reset input pin.

MC20 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 1 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 1)	No Change	No Message Info Word is written	None

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
T/$\overline{R}$ bit equals 1 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR
T/$\overline{R}$ bit equals 1 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word not followed by a contiguous data word (missing data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. WCTERR bit updated. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Mode code command word followed by data word with Manchester encoding or parity error (bad data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. IWDERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

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*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
OVERRIDE SELECTED TRANSMITTER SHUTDOWN (MC21): Mode code command with mode code 10101 and T/$\overline{R}$ bit equals 0	Default response: Reset Message Error (ME) status. and transmit Status Word. If broadcast, set the BCR status bit and suppress Status response.	DBAC bit reset. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA

After Status Word transmission, the device stores received data word in the assigned index or ping-pong buffer (or in Descriptor Word 4 if SMCP Simplified Mode Command Processing applies).

If the MCOPT4 bit in Configuration Register 2 equals 0, the received data word is compared to the value in the Bus Select Register corresponding to the inactive bus. For example, if the command is received on Bus A, the comparison uses the Bus B Select Register value. If the compared values match, the device automatically re-enables **transmit and receive** for the inactive bus, regardless of the state of the SDSEL bit in Configuration Register 2. The device affirms fully reenabled bus status by resetting all four TXASD, TXBSD, RXASD and/or RXBSD bits in the Built-In Test Register at register address 0x0014. Note: If the TXINHA or TXINHB input pins are asserted, the device cannot override the resulting hardware transmit inhibit for the affected bus. In this case, the corresponding TXASD and/or TXBSD bits remain high. See Built-In Test Register description for further information.

If MCOPT4 bit in Configuration Register 2 equals 0, the IWA interrupt is typically used to alert the host when an MC21 command is received. **The host** must evaluate whether the received mode data word matches the bus selection criteria. If bus selection criteria is met, **the host** fulfills the “override shutdown” command using one of two options:

1. reset the bus shutdown bit INHBUSA or INHBUSB for the inactive bus in Configuration Register 1 to reenable both transmit and receive, if the host used this bit to shut down transmit and receive for an earlier MC4 or MC20 command. (Resetting this shutdown bit does not restore bus transmit capability if a TXINHA or TXINHB input pin is asserted.)

OR

2. reset the transmit shutdown input pin TXINHA or TXINHB for the inactive bus to re-enable transmit if the host used this pin to shut down transmit only for an earlier MC4 or MC20 command.

MC21 EXCEPTIONS:				
Invalid command word. **OR** T/$\overline{R}$ bit equals 1 and UMCINV bit in Config. Register 1 equals 1 ***	No terminal response, the message is ignored. No Status Word change. (mode code is undefined when T/$\overline{R}$ bit equals 1)	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 1 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 0 *	Respond “In form”: Reset Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, set the BCR status bit and suppress status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	IWA IBR

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
T/$\overline{R}$ bit equals 1 **AND** UMCINV bit in Config. Register 1 equals 0. The Illegalization Table bit equals 1 **	Set Message Error (ME) status. If not broadcast, transmit Status Word. If broadcast, also set Status Word BCR bit and suppress Status response.	DBAC bit set. BCAST bit updated. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA IBR
Mode code command word not followed by a contiguous data word (missing data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR
Mode code command word followed by data word with Manchester encoding or parity error (bad data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. IWDERR bit set. BUSID bit updated. ILCMD bit reset. RTRT bit reset. (Other error bits reset.)	MERR IWA IBR

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”
*** Undefined mode command rendered invalid by UMCINV option bit. Command’s bit in Illegalization Table is “don’t care”.

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
RESERVED MODE CODES MC22 - MC31: Mode code commands having mode codes 10110 through 11111	The reserved mode code commands do not have defined actions. Host must initialize device to respond using either of the two following methods:			
The mode code's bit in Illegalization Table equals 1 ** (RT is using "illegal command detection")	Mode code is illegalized. Set Message Error (ME) status and transmit Status Word. If T/$\overline{R}$ bit equals 1, suppress data word transmission.	DBAC bit set. BCAST bit reset. DPB bit toggles.	ILCMD bit set. MERR bit set. BUSID bit updated. RTRT bit reset. (Other error bits reset.)	ILCMD IWA
OR	**OR**			
The mode code's bit in Illegalization Table equals 0 * (RT not using "illegal command detection," respond "in form")	**If T/$\overline{R}$ bit equals 1,** Reset Message Error (ME) status. Transmit Status Word with contiguous data word read from assigned index or ping-pong buffer (or from Descriptor Word 4 if the SMCP option applies.)	DBAC bit set. BCAST bit reset. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset. (All error bits reset.)	IWA
	If T/$\overline{R}$ bit equals 0, Reset Message Error (ME) status and transmit Status. If broadcast, also set BCR status and suppress Status transmit. Device stores received data word in assigned index or ping-pong buffer (or in Descriptor Word 4 if SMCP Simplified Mode Command Processing applies).	DBAC bit reset. BCAST bit updated. DPB bit toggles.	Normal CS update: BUSID bit updated. MERR bit reset. ILCMD bit reset. RTRT bit reset (All error bits reset.)	IWA IBR
MC22 - MC31 EXCEPTIONS:				
Invalid command word.	No terminal response, the message is ignored. No Status Word change.	No Change	No Message Info Word is written	None
T/$\overline{R}$ bit equals 0 and mode code command word is not followed by a contiguous data word (missing data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. WCTERR bit set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA IBR

Circumstances for Received Message	Terminal Response to Received Command	Bits Updated in Descriptor Control Word	Bits Updated in Data Buffer Msg Info Word	Interrupt Options
T/$\overline{R}$ bit equals 0 and command word is followed by data word with Manchester or parity error (bad data word)	No Status Word transmit. Set the Message Error (ME) status bit. If broadcast, set the BCR status bit.	DBAC bit set. BCAST bit updated. DPB bit toggles.	MERR bit set. IWDERR bit set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA IBR
T/$\overline{R}$ bit equals 1 and mode code command word is followed by a contiguous data word	No Status Word transmit. Set the Message Error (ME) status bit.	DBAC bit set. BCAST bit reset. DPB bit toggles.	MERR, WCTERR bits set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA
T/$\overline{R}$ bit equals 1 and mode code command is addressed to RT31	No Status Word transmit. Set the Message Error (ME) and BCR status bits.	DBAC bit set. BCAST bit set. DPB bit toggles.	MERR bit set. BUSID bit updated. ILCMD, RTRT bits reset. (Other error bits reset.)	MERR IWA IBR

* Command is illegal but terminal is not using “illegal command detection” (in form response).
** Command is illegal and terminal is using “illegal command detection”

17. ELECTRICAL CHARACTERISTICS

17.1. Absolute Maximum Ratings

Supply voltage (V_{DD})	-0.3 V to +5.0 V
Logic input voltage range	-0.3 V to +3.6 V
Receiver differential voltage	10 Vp-p
Power dissipation at 25°C	1.0 W
Reflow Solder Temperature	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

17.2. Recommended Operating Conditions

Operating Supply voltage (V_{DD})	3.3 VDC ± 5%
Operating Temperature Range	
Industrial Extended	-40°C to +85°C -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

17.3. DC Electrical Characteristics

V_{DD} = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Operating Voltage	V_{DD}		3.15	3.3	3.45	V
Power Supply Current See Note 1 on next page	I_{CC1}	Not Transmitting	-	4	10	mA
	I_{CC2}	Continuous supply current while one bus transmits @ 100% duty cycle, 70Ω resistive load	-	720	760	mA
Power Dissipation See Note 2 on next page	PD_1	Not Transmitting	-	-	60	mW
	PD_2	Transmit one bus @ 100% duty cycle, 70Ω resistive load	-	420	550	mW
Input Voltage (HI)	V_{IH}	Digital Inputs	70%	-	-	V_{DD}
Input Voltage (LO)	V_{IL}	Digital Inputs	-	-	30%	V_{DD}
Input Current (HI)	I_{IH}	Digital Inputs	-	-	20	µA
Input Current (LO)	I_{IL}	Digital Inputs	-20	-	-	µA
Pull Up / Pull Down Current	I_{PUD}	Digital Inputs and Data Bus	-	275	-	µA
Output Voltage (HI)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs	90%	-	-	V_{DD}
Output Voltage (LO)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs	-	-	10%	V_{DD}
RECEIVER (Measured at Point "AD" in Figure 26 unless otherwise specified)						
Input Resistance	R_{IN}	Differential	20	-	-	kΩ
Input Capacitance	C_{IN}	Differential	-	-	5	pF
Common Mode Rejection Ratio	CMRR		40	-	-	dB
Input Level	V_{IN}	Differential	-	-	9	Vp-p

Parameters		Symbol	Test Conditions	Limits			Unit
				Min	Typ	Max	
Input Common Mode Voltage		V_{ICM}		-5	-	+5	V-pk
Threshold Voltage (Direct-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "AD" in Figure 26)	1.15	-	20.0	Vp-p
	No Detect	V_{THND}		-	-	0.28	Vp-p
Threshold Voltage (Transformer-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "AT" in Figure 27)	0.86	-	14.0	Vp-p
	No Detect	V_{THND}		-	-	0.2	Vp-p
TRANSMITTER (Measured at Point "AD" in Figure 26 unless otherwise specified)							
Output Voltage	Direct Coupled	V_{OUT}	35Ω Load	6.6	-	9.0	Vp-p
	Transformer Coupled	V_{OUT}	70Ω Load (Measured at Point "AT" in Figure 27)	20.0	-	27.0	Vp-p
Output Noise		V_{ON}	Differential, inhibited	-	-	10.0	mVp-p
Output Dynamic Offset Voltage	Direct Coupled	V_{DYN}	35Ω Load	-90	-	90	mV
	Transformer Coupled	V_{DYN}	70Ω Load (Measured at Point "AT" in Figure 27)	-250	-	250	mV
Output Resistance		R_{OUT}	Differential, not transmitting	10	-	-	kΩ
Output Capacitance		C_{OUT}	1 MHz sine wave	-	-	15	pF

Note 1: In actual use, the highest practical transmit duty cycle is 96%, occurring when a Remote Terminal responds to a series of 32 data word transmit commands (RT to BC) repeating with minimum intermessage gap of 4µs (2µs dead time) and typical RT response delay of 5µs.

Note 2: While one bus continuously transmits, the power delivered by the 3.3V power supply is 3.3V × 720mA typical = 2.4W. Of this, 420mW is dissipated in the device, the remainder in the load.

17.4. AC Electrical Characteristics — HI-6121 Host Bus Interface Timing

V_{DD} = 3.3V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
HI-6121 INTERFACE TIMING (SPI Host Bus Interface)					
SCK clock Period	t_{CYC}	50	-	-	ns
$\overline{CE}$ set-up time to first SCK rising edge	t_{CES}	25	-	-	ns
$\overline{CE}$ hold time after last SCK rising edge	t_{CEH}	25	-	-	ns
$\overline{CE}$ inactive between SPI instructions	t_{CPH}	100	-	-	ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10	-	-	ns
SPI SI Data hold time after SCK rising edge	t_{DH}	10	-	-	ns
SO valid after SCK falling edge	t_{DV}	-	-	20	ns
SO high-impedance after $\overline{CE}$ inactive	t_{CHZ}	-	-	75	ns

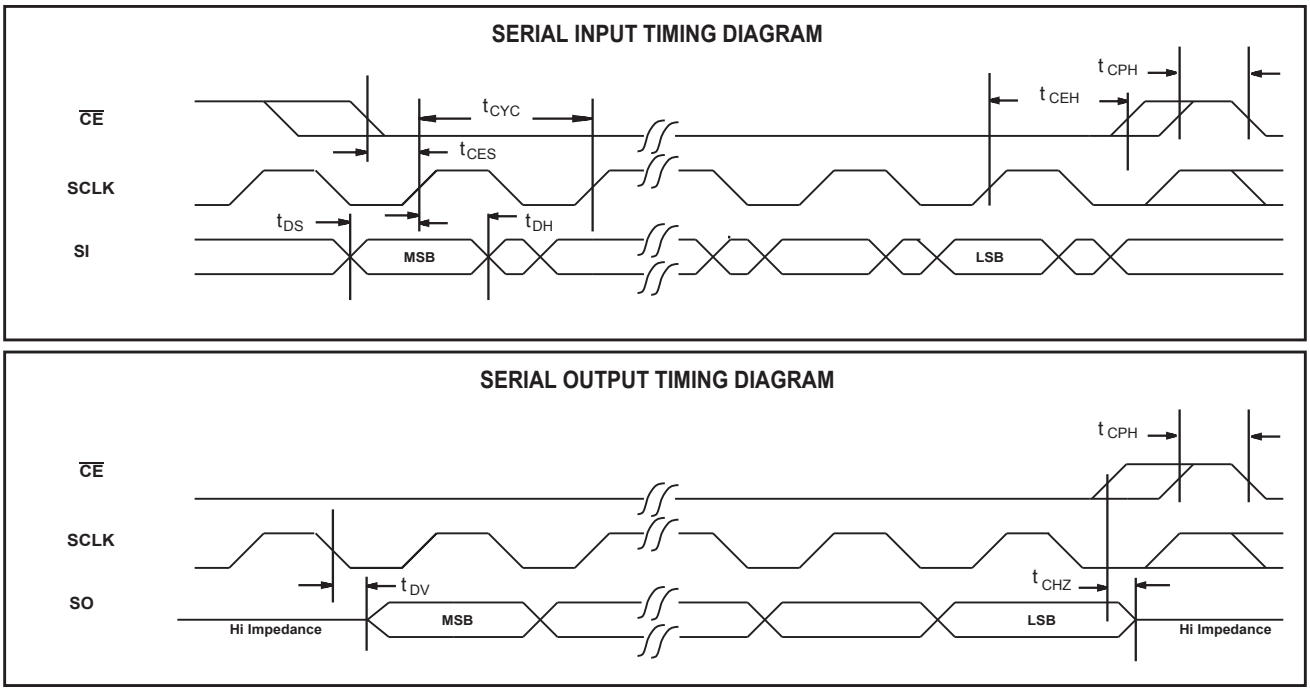
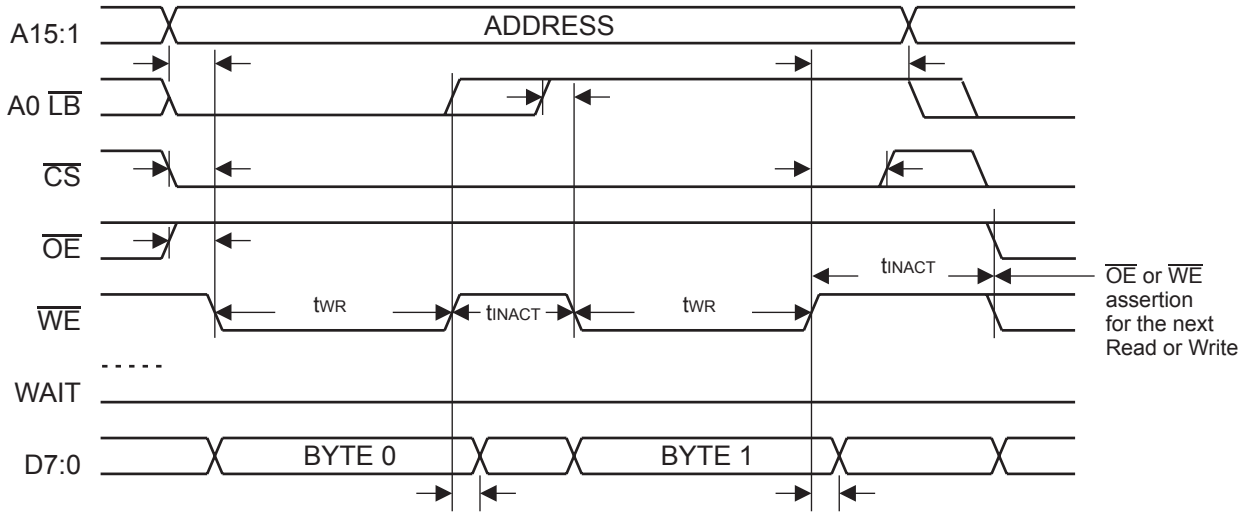


Figure 21. HI-6121 Host Bus Interface Timing Diagram

17.5. AC Electrical Characteristics — HI-6120 Host Bus Interface Timing

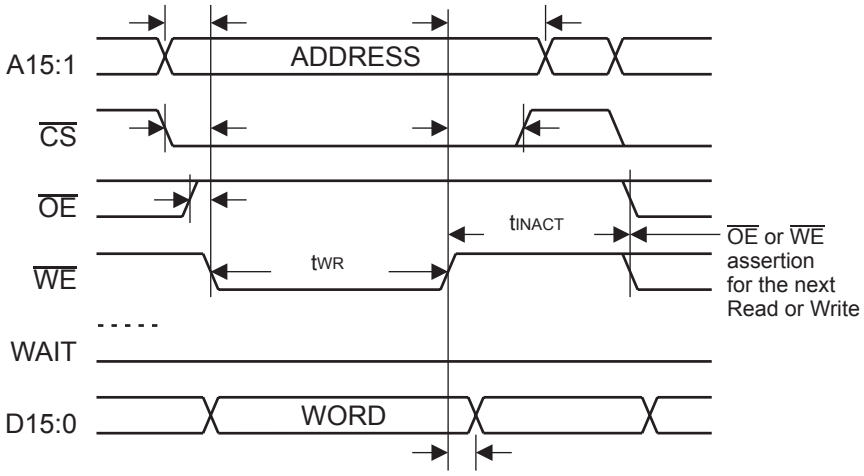
Parameters	Symbol	Limits			Units
		Min	Typ	Max	
HI-6120 INTERFACE TIMING (Parallel Host Bus Interface)					
Write cycle	t_{WR}	55	-	-	ns
Read/Write inactive time	t_{INACT}	25	-	-	ns
Non-sequential read time	t_{NSR}	110	-	-	ns
8-bit sequential read time	t_{SR8}	55	-	-	ns
16-bit sequential read time	t_{SR16}	65	-	-	ns
Wait assertion time	t_{WAS}	20	-	-	ns
Wait time	t_{W}	-	-	130	ns

HOST WRITE IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 1 (“Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)
showing 2 bytes written for a single 16-bit word



All timing intervals equal 0 ns MIN unless otherwise indicated.

HOST WRITE IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 1 (”Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)
showing a one-word write cycle. Successive writes to sequential addresses have same timing.

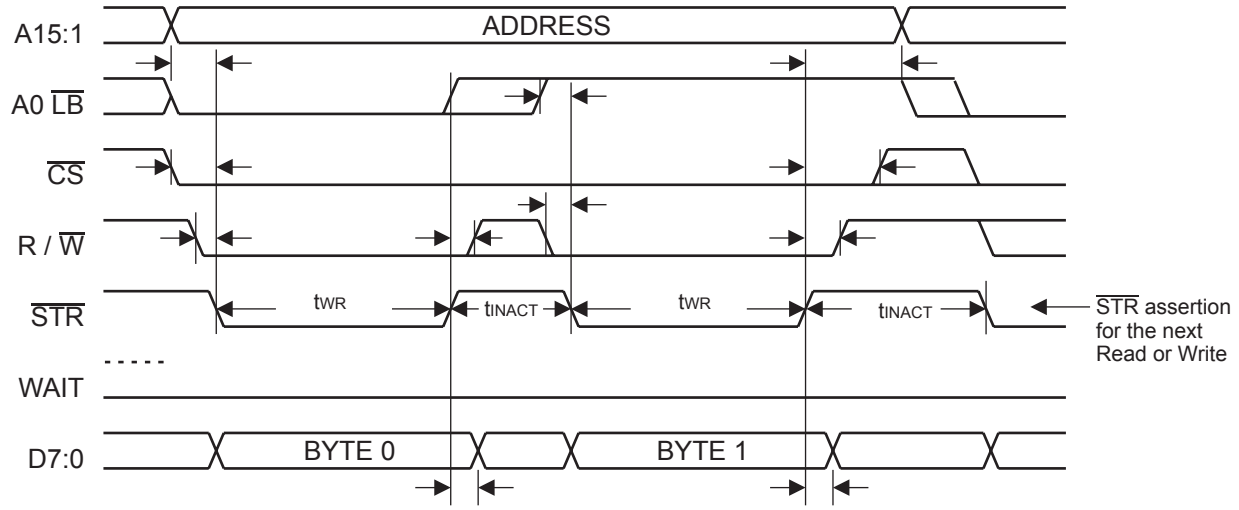


All timing intervals equal 0 ns MIN unless otherwise indicated.

Figure 22. Register and RAM Write Operations for BTYPE = 1

HOST WRITE IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

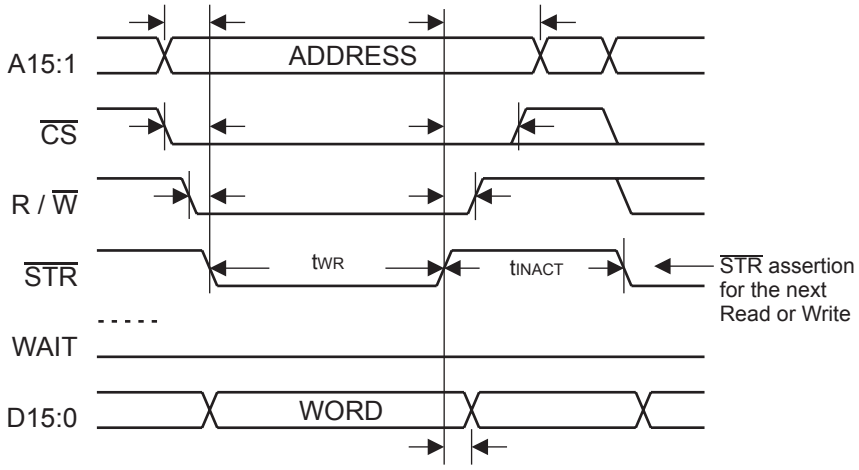
showing 2 bytes written for a single 16-bit word



All timing intervals equal 0 ns MIN unless otherwise indicated.

HOST WRITE IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

showing a one-word write cycle. Successive writes to sequential addresses have same timing.

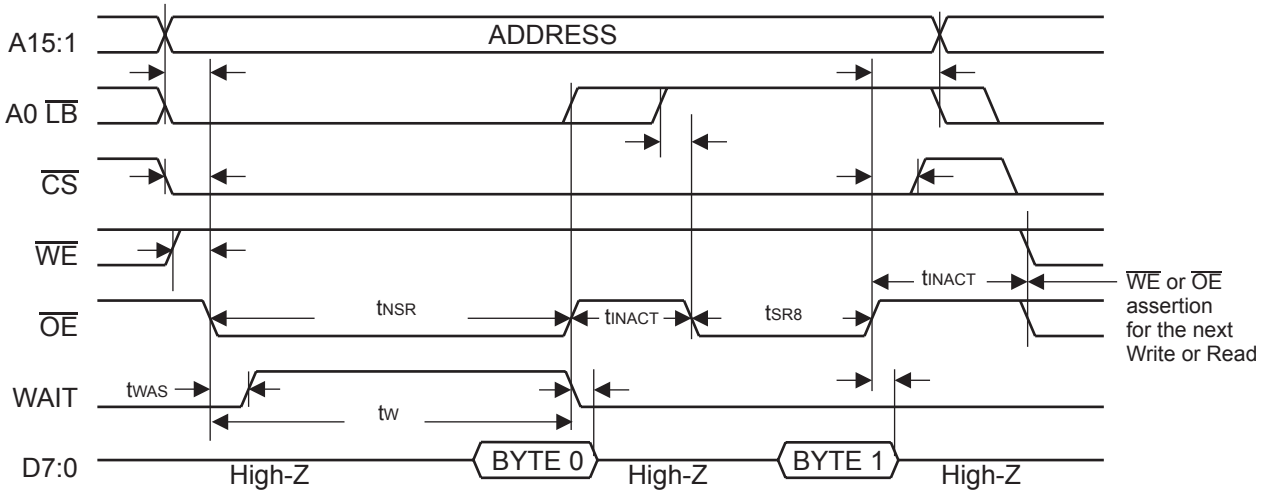


All timing intervals equal 0 ns MIN unless otherwise indicated.

Figure 23. Register and RAM Write Operations for BTYPE = 0

HOST READ IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 1 (”Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)

showing 2 bytes read for a single 16-bit word



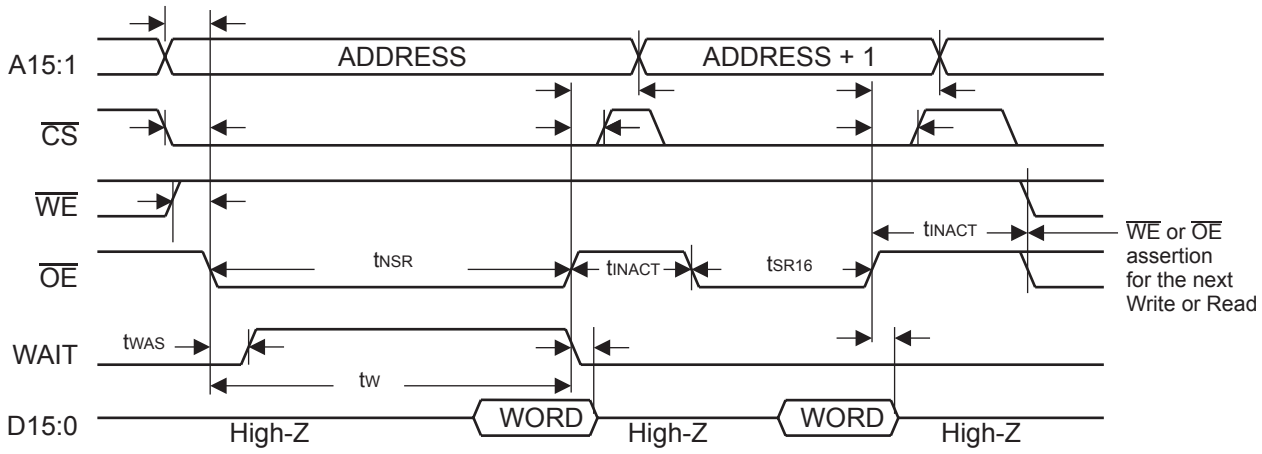
All timing intervals equal 0 ns MIN unless otherwise indicated.

After first byte is read, prefetch allows faster access times for successive reads, as long as addresses are sequential.

WAIT is always asserted during the first read cycle, is never asserted for successive read cycles to sequential adresses. This allows default host bus configuration for the HI-6120 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted.

HOST READ IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 1 (”Intel Style” - $\overline{OE}$ Output Enable and $\overline{WE}$ Write Enable)

showing two successive words read from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

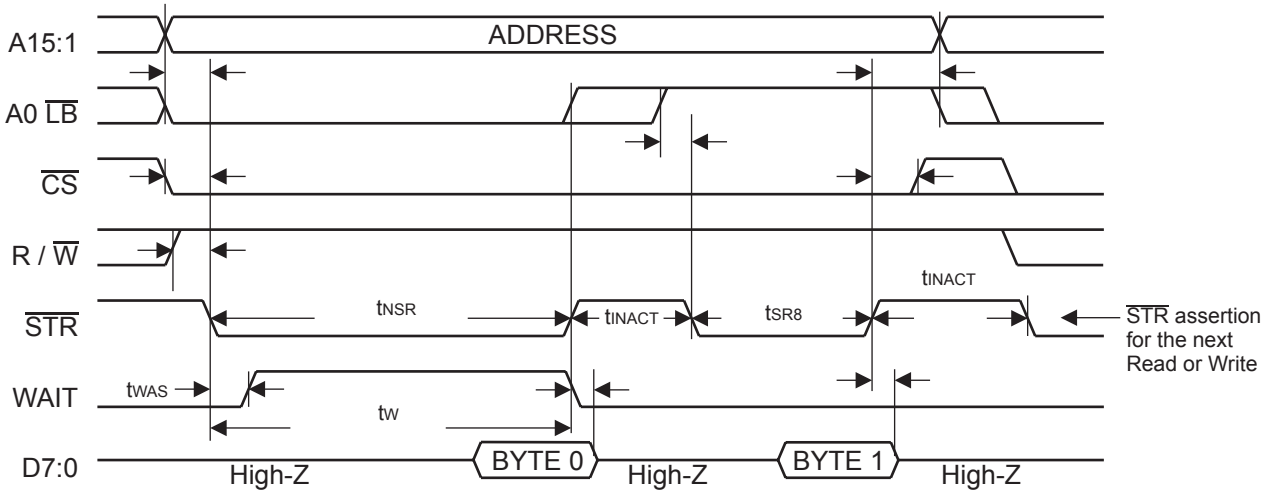
After first word is read, prefetch allows faster access times for successive reads, as long as addresses are sequential.

WAIT is always asserted during the first read cycle, is never asserted for successive read cycles to sequential adresses. This allows default host bus configuration for the HI-6120 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted.

Figure 24. Register and RAM Read Operations for BTYPE = 1

HOST READ IN DUAL-BYTE MODE (8-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

showing 2 bytes read for a single 16-bit word



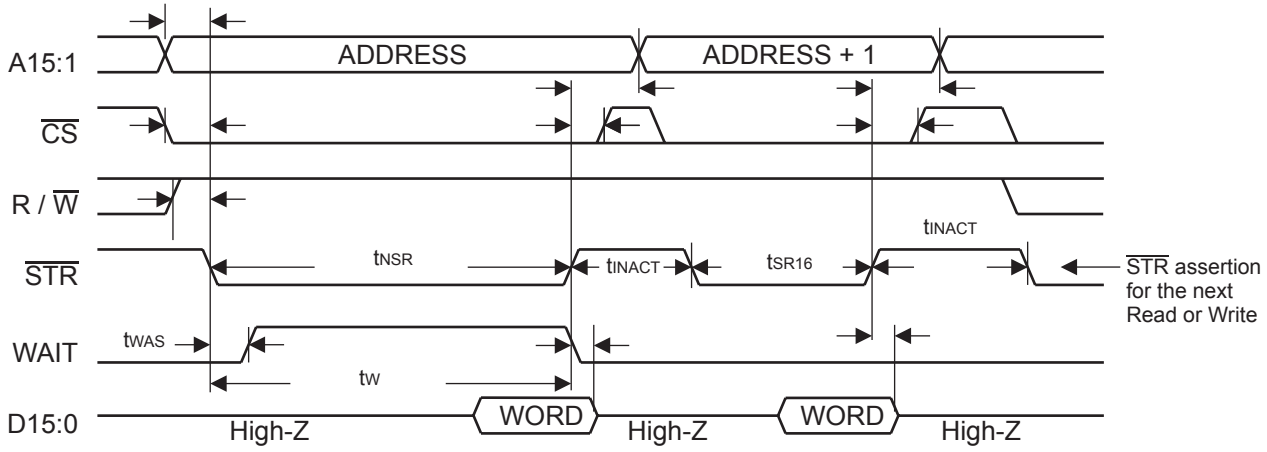
All timing intervals equal 0 ns MIN unless otherwise indicated.

After first byte is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential.

WAIT is always asserted during the first read cycle, is never asserted for successive read cycles to sequential adresses. This allows default host bus configuration for the HI-6120 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted.

HOST READ IN WORD MODE (16-BIT BUS WIDTH)
using BTYPE = 0 (”Motorola Style” - Single Read/Write Strobe $\overline{STR}$ and R/$\overline{W}$ Direction Select)

showing two successive words read from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

After first word is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential.

WAIT is always asserted during the first read cycle, is never asserted for successive read cycles to sequential adresses. This allows default host bus configuration for the HI-6120 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted.

Figure 25. Register and RAM Read Operations for BTYPE = 0

18. MIL-STD-1553 BUS INTERFACE

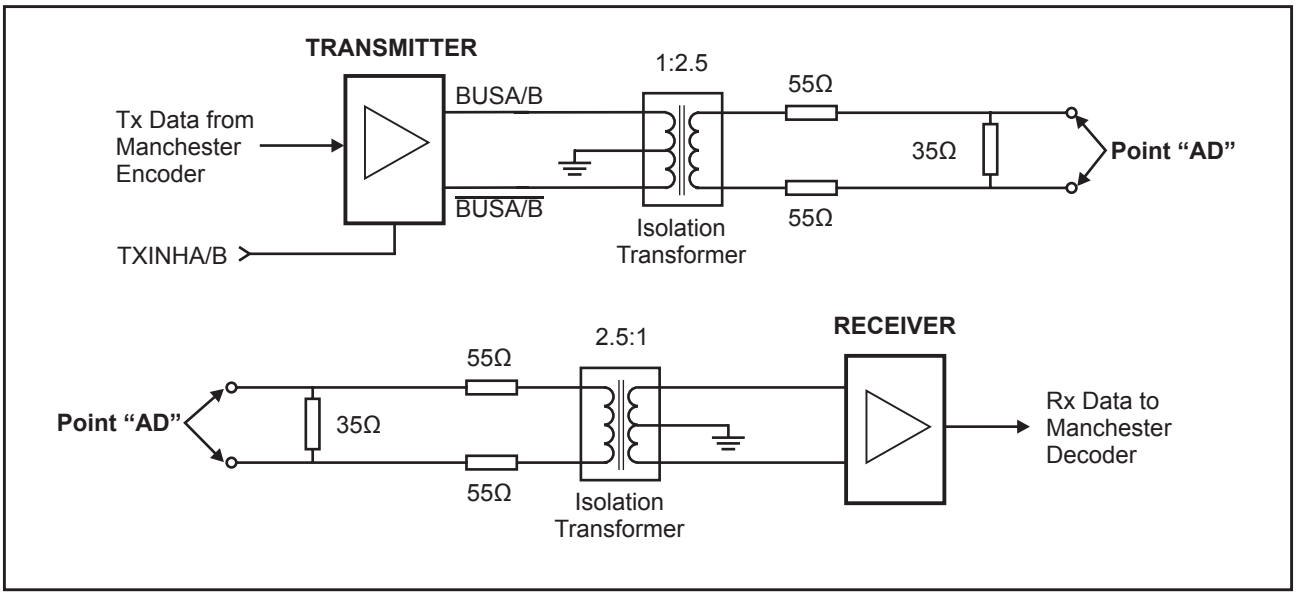


Figure 26. MIL-STD-1553 Direct Coupled Test Circuits

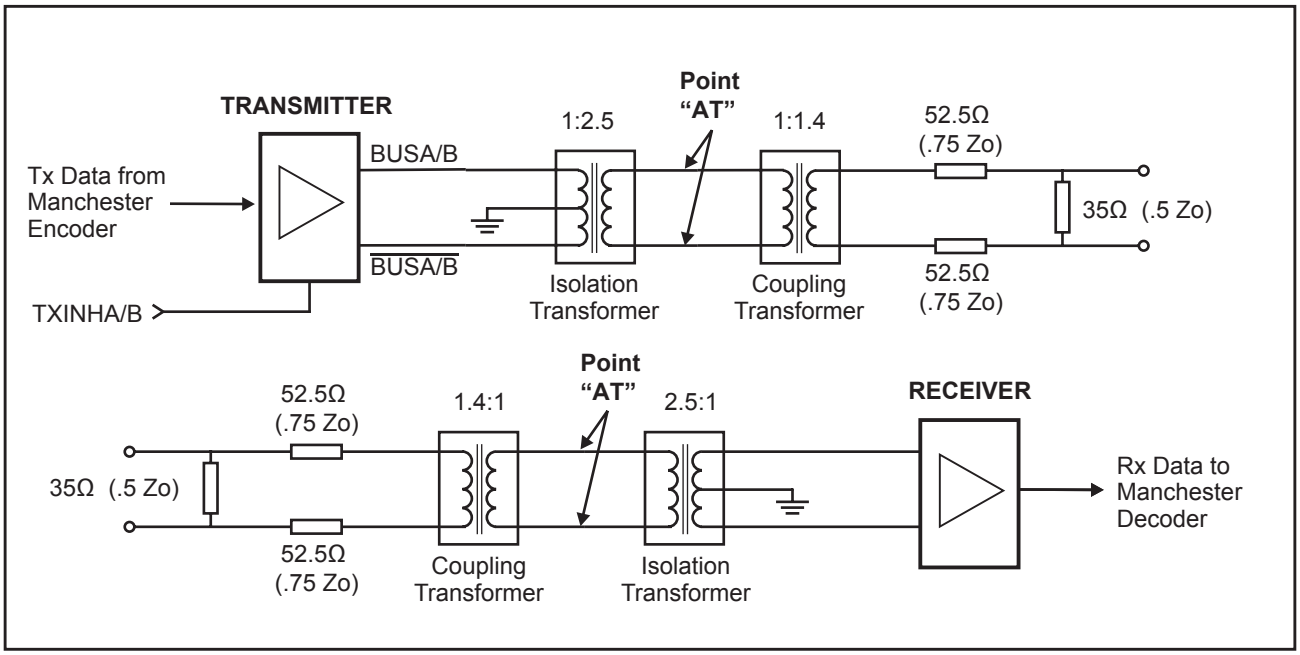


Figure 27. MIL-STD-1553 Transformer Coupled Test Circuits

19. RECOMMENDED TRANSFORMERS

The HI-6120 and HI-6121 integrated transceivers have been characterized for compliance with the electrical requirements of MIL-STD-1553 when used with the following transformers. Holt recommends the Premier Magnetics parts as offering the best combination of electrical performance, low cost and small footprint.

Manufacturer	Part Number	Application	Turns Ratio(s)	Dimensions
Premier Magnetics	PM-DB2702	Stub coupling	1:1.4	0.625 x 0.625 x 0.250 inches
Premier Magnetics	PM-DB2791S	Isolation	1:2.5	0.4 x 0.4 x 0.185 inches
Premier Magnetics	PM-DB2762	Isolation	Dual core stacked 1:2.5	0.4 x 0.4 x 0.320 inches
Premier Magnetics	PM-DB2776	Isolation	Dual core 1:2.5	0.675 x 0.4 x 0.185 inches

20. THERMAL CHARACTERISTICS

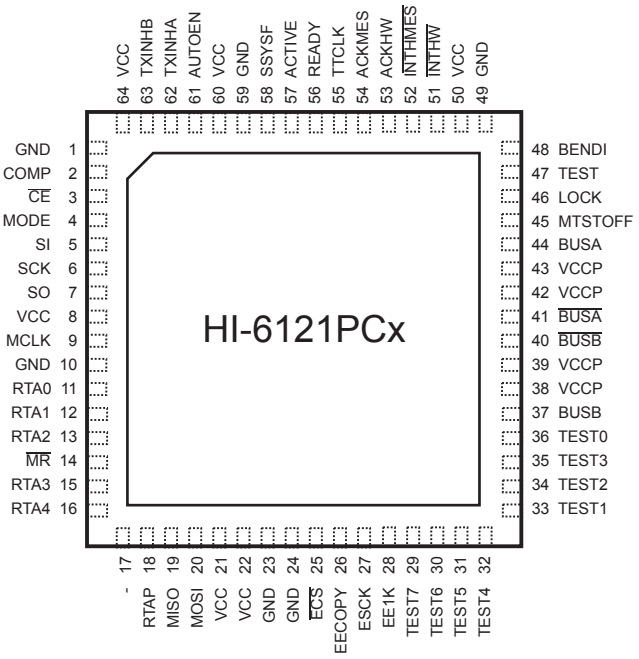
Part Number	Package Style	Condition	θ_{ja} (°C/W)	Junction Temp, T_j (°C)		
				T_A = 25°C	T_A = 85°C	T_A = 125°C
HI-6120PQx	100-pin PQFP	Mounted on circuit board	52.7	56	116	156
HI-6121PQx	52-pin PQFP	Mounted on circuit board	60.9	56	116	156
HI-6121PCx	64-pin QFN	Heat sink pad unsoldered	31.1	41	101	141
		Heat sink pad soldered	22.8	37	97	137

21. ADDITIONAL PIN / PACKAGE CONFIGURATIONS

Notes:

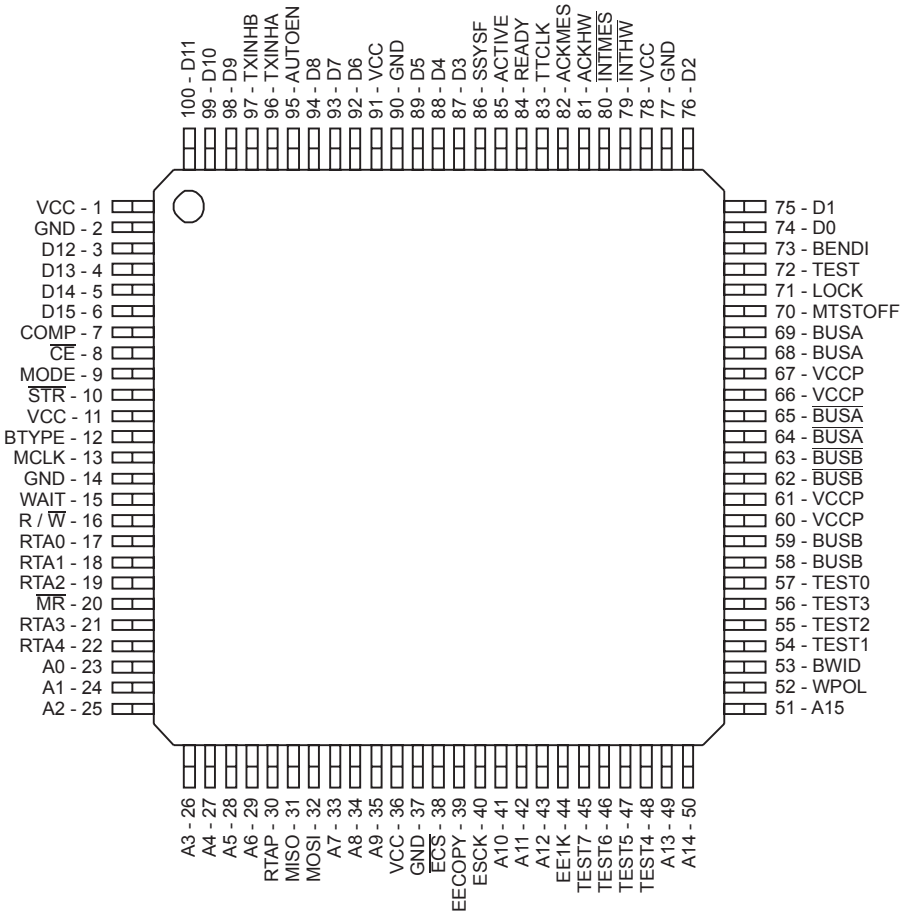
1. All VCC, VCCP and GND pins must be connected.
2. See page 1 for HI-6121, 52-Pin PQFP Package Configuration.

21.1. HI-6121PCx (64-pin QFN)



TOP VIEW

21.2. HI-6120PQx (100-pin PQFP)



TOP VIEW

22. ORDERING INFORMATION

HI - 6120 PQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PQ	100 PIN PLASTIC QUAD FLAT PACK, PQFP (100PQS)

HI - 6121 PQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PQ	52 PIN PLASTIC QUAD FLAT PACK, PQFP (52PQS)

HI - 6121 PC x x

PART NUMBER	LEAD FINISH
Blank	NiPdAu
F	NiPdAu (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PC	64 PIN PLASTIC CHIP-SCALE PACKAGE, 9 x 9mm QFN (64PCS)

23. REVISION HISTORY

Revision	Date	Description of Change
DS6120, Rev. NEW	11/24/09	Initial Release
Rev. A	6/15/10	Datasheet format change (Table of Contents, List of Figures, List of Tables and cross-references added). Inserted new sections to clarify Data Prefetch operations. Minor typos corrected.
Rev. B	11/18/10	Corrected Power Supply Current and device Power Dissipation values and added explanatory notes.
Rev. C	6/5/12	In Section “10.4. Receive Mode Command Control Word” on page 64, replaced “mode control word” with “Mode command control word”. In SMCP bit diagram, changed bit 8 from “PPON” to “Not Used”. In Section “10.5. Transmit Mode Command Control Word” on page 66, replaced “mode control word” with “Mode command control word”. In SMCP bit diagram, changed bit 8 from “PPON” to “Not Used”. Clarified text in “12.5. Simplified Mode Command Processing” on page 100. Corrected SPI clock rate from 16MHz to 20MHz on p. 109. Clarified description of command op code 0x60 in Section “15.2.6. Special Purpose Commands” on page 112. Clarified description of command op code 0x58 in Section “15.2.6. Special Purpose Commands” on page 113. Clarified description of op codes 0x60 and 0x58 in “Table 15. SPI Commands using Address Pointer Register” on page 119. Corrected value of t_{SCKL} in “17.4. AC Electrical Characteristics — HI-6121 Host Bus Interface Timing” on page 148 from 100ns to 25ns. Added Section “19. Recommended Transformers” on page 155. Updated 52 lead PQFP package dimensions. Clarified that reading the Pending Interrupt Register does not clear the interrupt outputs in “level” mode. See Sections “5.7. Pending Interrupt Register (0x0006)” on page 31 and “13.2. Host Interrupt Generation” on page 101.
Rev. D	02/26/14	Corrected units of current in DC Electrical Characteristics table. Clarified Reflow Solder Temperature in Absolute Maximum Ratings Table. Updated PQFP-52, QFN-64 and PQFP-100 package drawing units. Corrected error in pin-out of HI-6120PQx, HI-6121PCx and HI-6121PQx (pins TEST3 and TEST1 reversed on drawing). Added section for MIL-STD-1760 use: “MIL-STD-1760: Busy Status Assertion After Power-Up” on page 109.
Rev. E	06/04/14	Add additional bits to register “Configuration Register 2 (0x0001)” on page 24 to describe newly added features. Update other sections referenced and impacted by these changes.
Rev. F	07/24/14	Correct BCAST flag assertion in message information word.
Rev. G	10/30/14	Fixed minor typographical errors.
Rev. H	12/15/14	Update Transmitter Output Voltage in “DC Electrical Characteristics” on page 147 to comply with MIL-STD-1760 specification.

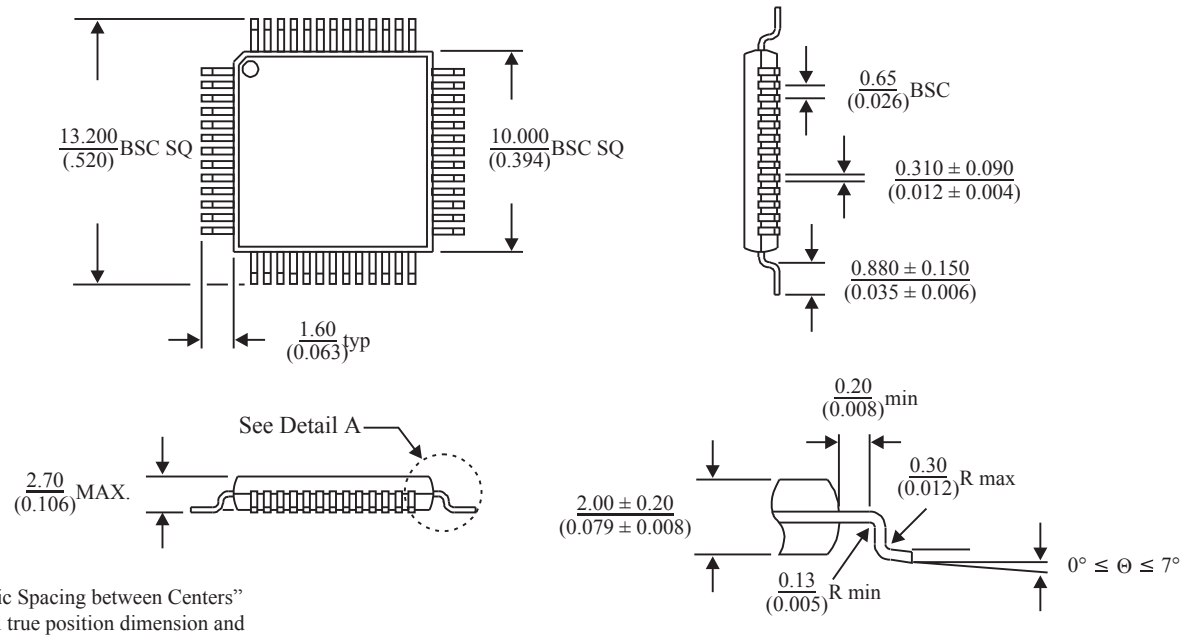
Rev. I	11/12/15	Correct SPI operation modes for EEPROM programming. Indicate t_{CYC} on Serial Input Timing Diagram. Correct Serial Output Timing Diagram for t_{CHZ} parameter. Remove t_{SCKH} and t_{SCKL} parameters. Correct other minor typos.
Rev. J	08/31/17	Clarify sequence of writing “Configuration Register 1 (0x0000)” during configuration, (specifically STEX bit), to ensure proper terminal configuration and start.
Rev. K	11/10/17	Clarify operation of BENDI, A0 and BWID pins; see Table 4 and Section “15.1. HI-6120 Host Bus Interface” for further details.
Rev. L	06/03/2021	Correct typos in “Appendix: RT Messages Responses, Options & Exceptions” for descriptions of MC17, MC20 and MC21. Clarify QFN lead finish of HI-6121PCx is NiPdAu.

24. PACKAGE DIMENSIONS

52-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 52PQS



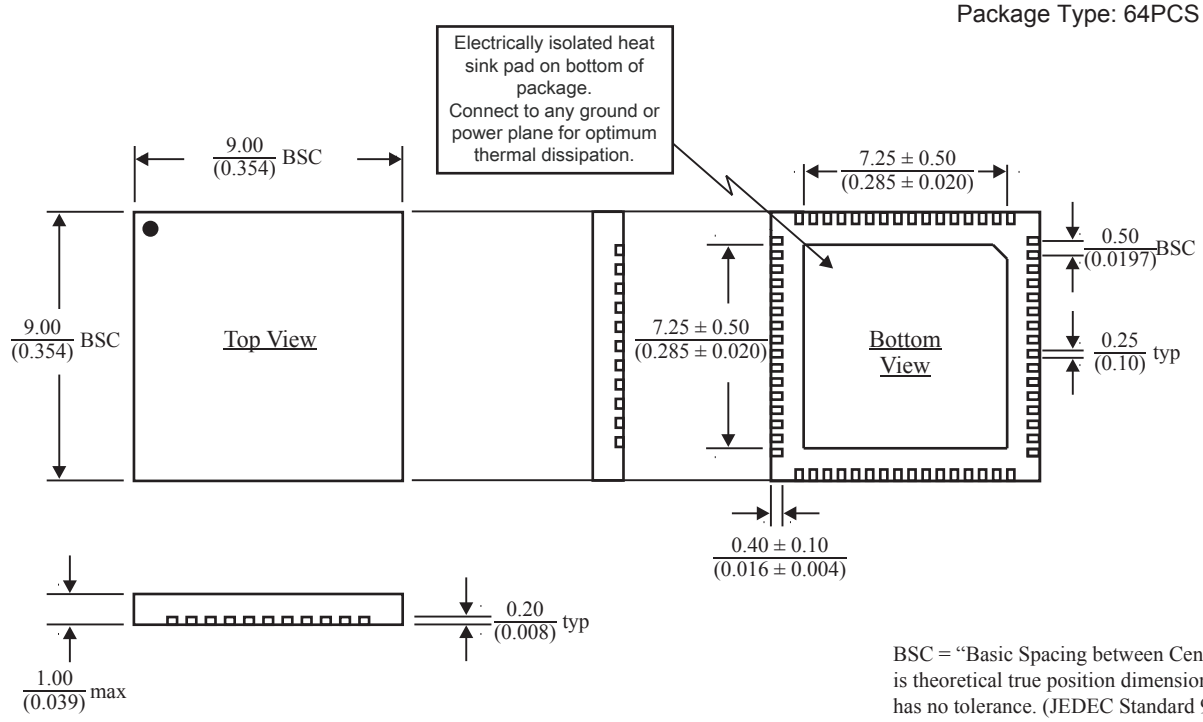
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

DETAIL A

64-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 64PCS

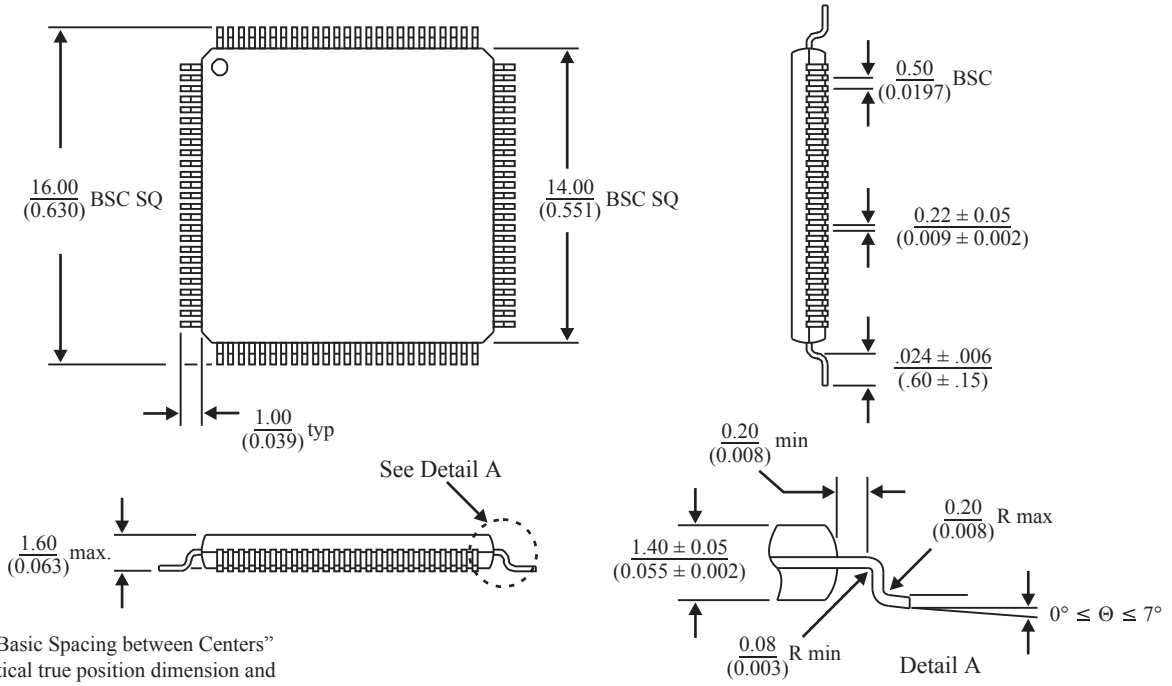


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

100-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 100PQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)